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IN THE UNITED STATES DISTRICT COURT

IN AND FOR THE EASTERN DISTRICT OF CALIFORNIA

CIV.S- 03 - 1329 WBS PAN

TECHNOLOGY LICENSING CORPORATION, a California corporation,	Case No.
Plaintiff,	COMPLAINT FOR PATENT INFRINGEMENT
v.	
THOMSON, INC., a Delaware corporation,	DEMAND FOR JURY TRIAL
Defendant.	

Plaintiff Technology Licensing Corporation ("TLC") files this complaint against defendant Thomson, Inc. ("Thomson") and alleges as follows:

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THE PARTIES

1. TLC is a corporation organized and existing under the laws of the State of California, with its principal place of business at 110 Knowles Drive, Los Gatos, California 95032-1828.

2. Thomson, on information and belief, is a corporation organized under the laws of the Delaware. Thomson is doing business in California and, on information and belief, has a place of business at 400 Providence Mine Road, Nevada City, California 95959. Thomson may be served with process by serving its registered agent, CT Corporation System, 818 West Seventh Street, Los Angeles, California 90017.

JURISDICTION & VENUE

3. This is an action for infringement of United States patents. Accordingly, this action arises under the patent laws of the United States of America, 35 U.S.C. §§ 1 *et seq.* and jurisdiction is properly based on Title 35 United States Code, particularly § 271, and title 28 United States Code, particularly § 1338(a).

4. Thomson, upon information and belief, transacts business in this judicial district by making using, selling, and/or offering to sell products, methods and/or systems as described and claimed in United States Patent No. 5,754,250 ("the '250 patent"), United States Patent No. 5,486,869 ("the '869 patent"), United States Patent No. 4,573,070 ("the '070 patent"),and United States Patent No. 5,459,524 ("the '524 patent"), the patents at issue in this lawsuit, and/or by conducting other business in this judicial district.

5. Venue is proper in this court under Title 28 United States Code §§ 1391(b) and 1400(b).

PATENT INFRINGEMENT COUNT

6. On May 19, 1998, the '250 patent, entitled "Synchronizing Signal Separating Apparatus and Method," was duly and legally issued to J. Carl Cooper. A true and correct copy of the '250 patent is attached hereto as Exhibit "A."

7. On January 23, 1996, the '869 patent, entitled "Synchronizing Signal Separating Apparatus and Method," was duly and legally issued to J. Carl Cooper. A true and correct copy of the '869 patent is attached hereto as Exhibit "B."

8. On February 25, 1986, the '070 patent, entitled "Noise Reduction System for Video Signals," was duly and legally issued to J. Carl Cooper. A true and correct copy of the '070 patent is attached as "Exhibit C."

9. On October 17, 1995, the '524 patent, entitled "Phase Modulation Demodulator Apparatus and Method," was duly and legally issued to J. Carl Cooper. A true and correct copy of the '524 patent is attached as "Exhibit D."

10. TLC is the assignee of all rights in the '869, '250, and '524 patents and the assignee of all rights in the commercial market for the '070 patent. At all times relevant hereto, TLC has had the sole right to sue and recover for past, present, and future infringement of the '250, '869, and '524 patents. At all times relevant hereto, TLC has had the sole right to sue and recover for past, present, and future infringement of the '070 patent as related to commercial markets.

11. Thomson, on information and belief, manufactures, uses and sells products with synchronization signal separation capabilities, including, but not limited to, the Thomson Grass Valley 8900FSS. On information and belief, Thomson has in the past

infringed, and continues to infringe directly, by inducement, and/or by contributing to the infringement of one or more claims of the '250 patent, including, but not limited to, claim 33 by manufacturing, using, and selling such products. On information and belief, Thomson has in the past infringed, and continues to infringe directly, by inducement, and/or by contributing to the infringement of one or more claims of the '869 patent, including, but not limited to, claims 27, 31, and 40 by manufacturing, using, and selling such products.

12. Thomson, on information and belief, manufactures, uses, and sells products with demodulation capabilities for recovering information content from a modulated signal, including, but not limited to, the Thomson Grass Valley 8960DEC. On information and belief, Thomson has in the past infringed, and continues to infringe directly, by inducement, and/or by contributing to the infringement of one or more claims of the '524 patent, including, but not limited to, claims 11, 27, and 41 by manufacturing, using, and selling such products.

13. Thomson, on information and belief, manufactures, uses, and sells products into the commercial market with noise reduction systems using adaptive filter systems, including, but not limited to, the Thomson Grass Valley 8960DEC. On information and belief, Thomson has in the past infringed, and continues to infringe directly, by inducement, and/or by contributing to the infringement of one or more claims of the '070 patent, including, but not limited to, claims 1-2, 9, 15, 17-18, 22-25, 38-39, and 42-43 by manufacturing, using, and selling such products.

14. On information and belief, Thomson will continue to infringe the '250, '869, '070, and '524 patents unless enjoined by this Court.

15. As a consequence of Thomson's infringing conduct complained of herein, TLC has been irreparably damaged to an extent not yet determined, and TLC will continue to be irreparably damaged by such acts in the future unless Thomson is enjoined by this Court from committing further acts of infringement.

16. The infringement of the '250, '869, '070, and '524 patents alleged above has injured TLC and, thus, TLC is entitled to recover damages adequate to compensate for Thomson's infringement, which in no event can be less than a reasonable royalty.

PRAYER FOR RELIEF

Wherefore, TLC prays for entry of judgment:

1. that Thomson has infringed one or more claims of the '250 patent, including, but not limited to, claim 33;

2. that Thomson has infringed one or more claims of the '869 patent, including, but not limited to, claims 27, 31, and 40;

3. that Thomson has infringed one or more claims of the '070 patent, including, but not limited to, claims 1-2, 9, 15, 17-18, 22-25, 38-39, and 42-43;

4. that Thomson has infringed one or more claims of the '524 patent, including, but not limited to, claims 11, 27, and 41;

5. that Thomson, its officers, agents, employees, representatives, successors, and assigns and those acting in privy or in concert with them be permanently enjoined from further infringement of the '250, '869, '070, and '524 patents;

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6. that Thomson account for and pay to TLC all damages caused by the infringement of the '250, '869, '070, and '524 patents, which by statute can be no less than a reasonable royalty;

7. that TLC be granted prejudgment and post-judgment interest on the damages caused to them by reason of Thomson's infringement of the '250, '869, '070, and '524 patents;

8. that TLC be granted its attorneys' fees in this action;

9. that costs be awarded to TLC; and,

10. that TLC be granted such other and further relief as the Court may deem just and proper under the current circumstances.

Dated: June 20, 2003

Respectfully submitted,

WEINTRAUB GENSHLEA CHEDIAK SPROUL
Law Corporation

By: _____
Audrey A. Millemann
State Bar No. 124954
Attorneys for Plaintiff
Technology Licensing Corporation

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DEMAND FOR JURY TRIAL

Plaintiff hereby demands a trial by jury.

Dated: June 20, 2003

Respectfully submitted,

WEINTRAUB GENSHLEA CHEDIAK SPROUL
Law Corporation

By: _____
Audrey A. Millemann
State Bar No. 124954
Attorneys for Plaintiff
Technology Licensing Corporation

and are therefore more available in market. Therefore, detailed product part numbers and nominal values of components are marked on the components of FIGS. 8–11. The operation principle and interconnection of the components of the circuitry shown in FIGS. 8–11 are corresponding to FIG. 1 and FIGS. 2–4 and one skilled in the art will be able to understand FIGS. 8–11 from the forgoing description and explanation. Thus, the description of FIGS. 8–11 is omitted here.

FIG. 12 shows a prior art HDTV video format waveform which utilizes a two level sync pulse and an 8 level digital data format. The Data+FEC (Forward Error Correction) 1203 is carried in analog form constrained to a number of discrete levels which levels are allowed to change periodically, most usually in response to a clock signal. It may be noted that the sync pulse in this signal is not the same type of sync pulse as found in typical NTSC or similar prior art systems. The sync pulses in NTSC type systems are used to facilitate horizontal and vertical scanning of the electron beam of the TV display whereas the sync pulses of the present system of FIG. 12 are used to facilitate the location and subsequent recovery of the data segment. It will be appreciated from the present disclosure that the invention described herein may be used to advantage with any type of synchronizing, locating or identifying pulse or arrangement of a known pattern or sequence.

The use of the analog constrained level type of data transmission for video signals was described for example in U.S. Pat. No. 4,665,431 issued May 12, 1987. In the '431 patent such a system is seen in FIGS. 2 and 3 where the constrained data carries audio or other related signals in the video waveform.

The waveform of FIG. 12 is typical of the HDTV terrestrial broadcast transmission system which is proposed for the United States. Note that the 8 possible levels which the data may take on are shown simultaneously, as if the figure were an oscilloscope display repetitively triggered to the sync pulse. In normal operation where only a single one of a data segment is displayed the data will be seen to trace a single pattern among the various levels, such as shown in FIGS. 2 and 3 of the prior art '431 patent.

FIG. 13 shows a prior art HDTV video format which utilizes a two level sync pulse and a 16 level digital data format. This waveform is typical of the terrestrial HDTV cable TV transmission system which is proposed for the United States. It will be understood that the combination of analog constrained level data and two level sync pulses as shown in FIGS. 12 and 13 is provided herein as examples of prior art video type signals with which the present invention may be used to facilitate improved synchronizing pulse separation, however the invention is not intended to be limited to only these two examples and may be utilized to advantage with any other system which utilizes two or more level synchronizing or identifying type pulses with analog or digital information carried therewith.

For the video signals of both FIG. 12 and 13, it is preferred to establish a known D.C. reference level for the signal and to provide data reference levels with which the particular level that a data bit occupies may be determined. Alternatively, it is possible to measure the D.C. level of the video type signal and adjust the reference levels accordingly. As the video type signal level changes the data reference levels will change in response thereto in order to maintain the proper relationship. It will be recognized that establishing a proper reference level is preferred to be accomplished by use of known components of the synchronizing portion of the signal, such as a sync tip or a sync blanking level. The use of the sync components is preferred, since those are the best known and most easily identified levels of the signal by virtue of the defined arrangement and known pattern of the waveform the pattern having a repetitive nature. It will also be recognized that for the signal of FIGS. 12 and 13 establishing proper reference levels is best performed by using both the sync tip and sync blanking level. The function of determining which particular level that a data bit occupies will be referred to herein as slicing and may be determined by establishing data reference levels to which the data waveform or signal may be compared by multiple comparators, although the term slicing as used herein will be used to encompass all circuits, steps and functions for performing this task of determining which data reference levels a data bit falls between or matches.

As an example, with respect to FIG. 12 it is seen that there are 8 possible data levels identified on the left scale as occurring at levels labeled −7, −5, −3, −1, +1, +3, +5, and +7. In order to identify which of these eight levels the video signal occupies at a particular time it can be seen that establishing data reference levels between the video levels, and comparing the video to those reference levels is desired. For the present example it can be seen that the reference levels may be established at −6, −4, −2, 0, +2, +4, and +6. In addition it may be desired to detect that video has exceeded the allowable range by adding thresholds of −8 and +8. The capability of such detection will allow data to be flagged as suspect for example in the event of noise impulses. The establishment of such reference levels is often complicated by the fact that the areas of information between sync pulses may very well change in amplitude and D.C. offset level during the segment.

In order to overcome this problem it is necessary to first establish or measure some known parameter at each end of the segment in order to be able to estimate the change during the segment. This process first requires identifying the segment by identifying or detecting the arrangement or sequence of the known occurrences or patterns of the sync or other identifier. The present invention provides for such identification by locating or detecting a first transition of a known direction and amplitude, and inspecting the first transition to see if it occurs in a proper relation to a second known occurrence. The second known occurrence may be another transition of a known direction and level, or the occurrence of a known level for a known time. The detection of the proper relation of the known occurrences is preferred to be made by delaying a signal marking the first occurrence for an amount equal to the expected arrival of the second occurrence and determining if the two are approximately coincident, thereby indicating the proper relationship. Further inspection may be made by including a third or more occurrences in the inspection to ensure proper relationships.

Once the locations of segments of video, data or other information are known by the above determination of the locations of arrangements of known patterns of identifiers, the levels of known parts of the patterns may be utilized to establish the levels of one or more references at the start and end of the segments. Once the start and end levels are known the references may be adjusted throughout the segment in order to facilitate recovery of the information for example by data slicing.

FIG. 14 shows an expanded diagram of a typical one of the syncs of FIG. 12 or 13, showing data segment ending data 1401, leading sync blanking 1402, sync falling or leading edge 1406, sync tip 1403 with sync tip level 1408, sync rising or trailing edge 1407, sync trailing blanking 1404

and data segment beginning data **1405**. Note in particular that the 50% level of the sync pulse is identified for each of the leading and trailing edge by **1406** and **1407** respectively. It may also be noted that the sync pulse is corrupted by the presence of residual carrier pilot and other interference shown as the broadening of the waveform. FIG. **15** shows a typical expanded diagram of a typical pair of single data segments separated by a single sync pulse. FIG. **15** shows the first data segment ending data **1501** which happens to occur at the lowest level, leading sync blanking **1502**, sync falling or leading edge **1506**, sync tip **1503** with leading sync tip level **1508** and average sync tip level **1509**, sync rising or trailing edge **1507**, sync trailing blanking **1504** and the second data segment beginning data **1505** which happens to occur at the highest level. Note in particular that the 50% level of the sync pulse is identified for each of the leading and trailing edge by **1506** and **1507** respectively, and that they are not the same level as shown in FIG. **14**. It may also be noted that the sync pulse of FIG. **15** is also corrupted by the presence of residual carrier pilot and other interference shown as the broadening of the waveform. The presence of the residual carrier pilot is of particular concern since if not properly accounted for it can upset the measurement of sync blanking and tip. It is desired that any sample and hold which is utilized to sample the level of a sync component have a sample period which is an integral multiple of cycles of this carrier in order that the effect of the carrier will be integrated out by the hold circuit. Alternatively, filtering of the sync component may be utilized.

It may be noted that the waveform of FIG. **15** is corrupted in a relatively low frequency manner, which is demonstrated for purposes of example by the tilt in the sync tip and the associated different levels of **1502** and **1504**, and also **1506** and **1507**. It will also be recognized that the amplitude of the overall waveform may be affected such as to change the overall amplitude, or to compress or expand portions of the amplitude in a nonlinear fashion. All of these various distortions may be experiences simultaneously in a static or time varying fashion.

Tilt will be used herein to signify any type of distortion of the video signal whereby the position of sync components and/or data components are disturbed within a single sync period or from period to period. This distortion may be caused for example by capacitive coupling of the video waveforms with the resulting average level which changes due to the data in the different data segments being at different levels. Other causes of distortion may include interference from unwanted signals being introduced into the video signal, or reflections of the signal itself from terrestrial objects or imperfect transmission either over the air, in the cable system or in the video transmitting, receiving or processing circuitry.

In establishing the reference levels for subsequent slicing of the data, it will be necessary to either first remove the tilt from the waveform, or to generate reference levels having the same tilt as the waveform. It is preferred to remove the tilt by clamping the waveform to a known D.C. level and to generate the required reference values in response to the amplitude of the sync pulse. It is further preferred to adjust the amplitude of individual ones of the reference values in response to the data itself in order to optimally place said reference values between the data levels. In this fashion the reception of the transmitted data of the video signal may be optimized.

FIG. **16** shows a diagram of the preferred embodiment of the present invention having a video input **1601** for receiving the video type signal, a processing circuit **1602** for receiving and processing the video type signal. Circuit **1602** is preferred to include common mode rejection capability and filtering to remove unwanted interference signals which are of a fixed frequency nature. The output of **1602** is coupled to a falling edge detector **1614** to a rising edge detector **1615**, and to a D.C. level adjustment circuit shown in this preferred embodiment as a resistor network **1604** and **1605**. It will be recognized that the output of **1602**, as well as any other of the signals at any other stage utilized in the invention, may be coupled in any fashion known to those of ordinary skill in the art, including capacitively coupled as shown by **1603**.

The falling edge detector **1614** operates to detect when a falling edge is present in the signal, such as the edge **1506** of FIG. **15**. The output of the falling edge detector may be considered a marking signal and the marking signal is delayed by an edge to edge delay **1616** where the delay is slightly shorter than the time period or number of clocks from the leading edge **1506** to the trailing edge **1507**. The rising edge detector **1615** operates to detect when a rising edge is present in the signal, such as the edge **1506** of FIG. **15**. It will be recognized that by the addition of a window level comparator to the coincidence detect **1617** that the presence and duration of a particular level of the sync signal may be detected. The detection of the duration of the sync tip **1503** is described above, and if the window detector is combined to verify that the level of sync tip is between two known levels then the level and duration of sync tip may be detected. Such detection is also possible for other levels such as the sync blanking level **1502** or **1504**.

It will thus be appreciated that events of transitions of known direction and amount as well as events of levels of known amount and time may be detected as well as the relationships of the events, including the sequence and timing of such events may be detected and utilized to detect or verify the occurrence of sync or other types of timing signals in the video type signal.

The edge detectors are preferred to take into account the distance the edge falls or rises such as by differentiating the edge to generate a spike, and comparing the amplitude of the spike to a reference such that edges which occur due to data transitions from one level to another which are smaller than the distance from sync pulse blanking **1502** to sync tip **1508** may be discarded. Thus only edge transitions equal to or greater than the substantial amplitude of sync edges are detected. Such an edge detector is implemented in **120** of FIG. **2** as previously described and is also shown in FIG. **20**.

As previously mentioned the delay **1616** delays the leading sync pulse by slightly less than the expected period of a legitimate sync pulse. The coincidence and period detector **1617** then checks to see if a leading pulse is followed at substantially the proper time or number of clocks by a trailing pulse. If so, the period detector then checks to see if this set of pulses occurred at the proper time or number of clocks after the preceding received set of pulses, which preceding set is delayed by period delay **1620**. In other words, **1617** checks for proper sync pulse width and period. It will be recognized that the detection of periods and delays may be performed by the use of time delays or clock period delays as one skilled in the art will be able to choose to fit a particular implementation of the invention without departing from the scope of the invention. In particular, the delays may be implemented with clock counters in order that they track transmission rate variations of the video type signal.

It is preferred that **1617** utilize some amount of windowing in checking for proper sync pulse period and width in

order to allow for small variations which may occur to legitimate syncs due to noise, time base errors, transmission imperfections and the like. This is the reason that delay **1616** is preferred to delay by an amount slightly less than the width of a sync pulse and detect as proper pulses which arrive between that time and a time slightly more than that of a proper sync pulse. In particular it is preferred that both the pulse width and pulse period detectors operate to detect within a window of 95% to 105% of the expected value.

While the pulse period delay is shown as being separately connected to **1616** to represent that it presents the previously detected pulse from **1616** and presents it to **1617** after a delay, it will be recognized that it may also be connected to the output of **1617**. The former case will allow quicker startup and acquisition and the latter will provide better noise immunity since any pulse out of **1617** will need to have been preceded by a pulse which occurred a pulse period earlier. It will be recognized however that if there is never a pulse out of **1617** upon initial startup, that there will never be a pulse from **1620**, thus causing **1617** to latch up. This condition must be detected and prevented. For example, **1620** can be connected to **1616** if there is no previous output from **1617** stored in **1620**, and then connected to **1617** as soon as there is an output from **1617**. This function may be performed by a simple retriggerable oneshot which sets when a pulse is received from **1617** and times out if no pulse is received after 1½ pulse periods. As long as the oneshot is triggered, the output of **1617** is used to feed **1620**. If the oneshot times out the output of **1616** feeds **1620**.

The output of **1617** is coupled to a sample pulse generator and PLL **1618**. The PLL is utilized to provide sample clocks and other clocking signals for subsequently sampling and clocking the data from the video signal, and for other clocking and timing functions as will be apparent to one of ordinary skill in the art. The sample pulse generator **1619** operates to provide properly times sample signals to the various sample and hold circuits to take samples of the video signal level at known times, for example to the sample switches **1608**, **1609** and **1610** to take samples of the sync pulse blanking levels **1502** and **1504** with switch **1608**, the high reference level which in the preferred embodiment is also **1502** and **1504** with switch **1609**, and sync tip level **1509** with switch **1610**. Other sample signals may be provided as well as will be discussed below.

Sample switch **1608** along with reference **1621**, negative integrator **1607** and current providing resistor **1605** operate to D.C. restore the video signal the same as that of circuit **110**. While not shown in FIG. **16**, it will be recognized that any of the additional functions provided in FIG. **1** may also be included in the circuit of FIG. **16** as desired.

Sample switches **1609** and **1610** operate in conjunction with high and low level hold circuits **1611** and **1612**, respectively, to sample and hold the levels of the sync pulse. In that the level of the sync pulse is directly related to the levels of the references between each of the data levels of the data segment, the data reference level circuit **1613** receives the levels from **1611** and **1612** in order to establish reference levels for data slicing, as shown in FIG. **17**.

In FIG. **17** the high level signal and low level signals from **1611** and **1612** are coupled to the reference level circuit at **1701** and **1702**, respectively. These levels are translated to the upper reference level and lower reference level by amplifiers **1703** and **1704** having respective gains A1 and A2. This translation may be appreciated by inspecting FIG. **13** where it can be seen that the upper level needs to be between the upper two data levels corresponding to 14 on the left scale whereas the high level of the sync pulse corresponds to level 9. Correspondingly, the sync tip is at level −9 and the lower reference level should be at −14.

The upper and lower reference levels are then divided into the multiple data reference levels necessary for data slicing by resistors **1705***a–n* as shown by way of example in FIG. **17**. As related to FIG. **13**, these reference levels would correspond to 15 values of 14, 12, 10, 8, 6, 4, 2, 0, −2, −4, −6, −8, −10, −12 and −14 on the left scale which values define 16 possible data words. It will be understood that while the operation of FIG. **17** is shown by way of example with respect to voltages and resistances, it may be provided by equivalent use of currents and current ratios as will be known to one of ordinary skill in the art.

Each reference level from the resistor network **1705** is coupled to a comparator **1706** with the data & FEC (Forward Error Correction) portion of the video signal coupled to the other inputs of all of the comparators via **1708**. The outputs of the 15 comparators are coupled to the combination logic **1707** which provides a combined digital output **1709** which represents a particular one of 16 words corresponding to the data level of the video at a particular time.

FIG. **18** shows a digital embodiment of the present invention. It will be recognized that many of the functions of the present invention may be performed in the digital domain rather than the analog domain which is described in respect to the preferred embodiment. The video is received at **1801**, processed by **1802** and coupled from **1802** to a sync separator **1812** which provides a coarse separation of sync, and may be comprised of appropriate portions of FIG. **16**. The sync separator provides separated sync pulses to the PLL **1811** which generates clocks for the A-D **1805** and Processor **1806**. Alternatively, the clocks may be generated from the data as is well known in the art, in which case **1812** will be replaced with a clock or data extraction circuit.

The processor **1806** may be of a general purpose type, for example a microprocessor which is programmed to perform the steps or equivalent functions described herein via software control, or may be of a more dedicated type such as a DSP IC or dedicated IC designed specifically for the task. All of these embodiments will be known to be of use to one of ordinary skill in the art from the teachings herein.

The video data and FEC from **1802** is coupled to a processing circuit **1802** where it is prepared for coupling to an A-D convertor **1805** via a D.C. restoration circuit comprised of **1803** and **1804** and portions of a processor circuit **1806**. The A-D **1805** receives the D.C. restored video and a sampling clock from PLL **1811**. The video is digitized by **1805** with the digital video being coupled to the processor **1806**.

The processor includes circuitry for sampling the sync blanking levels and sync tip, comparing the level to a reference and generating a correction for providing D.C. offset via connection **1809**. Alternatively, the output of the comparison within **1806** may be coupled to an integrator **1810** as previously described.

Processor **1806** further provides establishing thresholds and slicing the data in response to the thresholds as previously described in order to provide the data out **1807** corresponding to **1709** of FIG. **17**. The processor may also provide sync separation or data or clock separation as previously described with respect to **1812**, or may provide conditioned data to **1812**. Additionally, **1806** may be configured to provide additional functions such as those connected with the utilization of the data.

It will be appreciated that if an A-D convertor having sufficient range is employed, with suitable coupling such as

capacitive coupling, that the D.C. restoration may be eliminated and thresholds for slicing may be computed on the fly within processor **1806** in order that the thresholds are dynamically adjusted as data is received in order to accommodate various tilt distortions. In particular, the level of the thresholds may be computed at both ends of a data block and adjusted throughout the data block to facilitate slicing.

As an example, if the data block is 100 clocks long, and a given threshold starts at value 50 units and ends at value 60 units the threshold value may be adjusted upward by 0.1 unit per clock thus causing the threshold to ramp up to track the tilt in the data. Another threshold might start at value 200 units and ends at value 180 units with this threshold value being adjusted downward by 0.2 unit per clock thus causing the threshold to ramp down to track the tilt in the data. This ramping threshold may then also be further finely adjusted in response to the data itself within and even continuously throughout the data block in addition to adjustment just at the ends. Accordingly, all thresholds may be simultaneously adjusted in different amounts and in different patterns. This approach provides not only for handling overall tilt of the data block, but will inherently compensate for any nonlinear distortion since the actual data may be utilized and the thresholds independently adjusted throughout the data block.

As a further example of the usefulness of **1806**, the tilt of the data block may be corrected before or as part of the data slicing. As with the previous example where the given threshold starts at value 50 units and ends at value 60 units the data values may be adjusted downward by 0.1 unit per clock thus causing the tilt to be removed from the data in order that a fixed threshold may be used. Combinations of the two approaches may be utilized as well.

FIG. **19** shows an analog circuit for providing fine adjustment to the thresholds which are utilized by comparators **1706** of FIG. **17** in response to the data of the video type signal. The high level and low level signals are coupled to **1703** and **1704** to provide the top and bottom levels however each data value of the video from **1620** is sampled as soon as that data level is determined by **1707**.

For example, a given data level N is detected as being between two thresholds N and N−1 by **1707**, and the sample and hold corresponding to that level is caused to operate to sample and hold the actual data level. This operation continues for all data levels as the corresponding data is received, including for samples of data at levels N+1. It will be seen that by splitting the resistors **1705** corresponding to the thresholds above and below a particular data level, and coupling the actual sampled and held data level to the split resistors, that adjustment of the threshold values immediately above and below may be had. In this fashion, the threshold values may be adjusted to lie precisely in the middle of the data levels. This operation may of course be included in processor **1806** discussed above.

FIG. **20** shows a sync edge detection circuit which may be utilized for **1614** and **1615** of FIG. **16**. The video signal having a sync pulse characteristic such as shown by **2002** is coupled to a differential **2001** which outputs pulses shown as **2003** which have an amplitude which is in proportion to the amplitude of the edge of **2002**. The pulses are compared to two references which are preferred to be set at 85% of the amplitude of the pulse corresponding to a legitimate sync edge. The comparator, upon receiving a pulse equal to or in excess of the reference outputs a pulse the presence of which indicates a sync edge or possibly a data transition having a magnitude equal to or greater than that of the corresponding reference level. If desired, a second set of comparators may be included which have references of 115% of the amplitude of the pulse corresponding to a legitimate sync edge. The comparator, upon receiving a pulse equal to or in excess of this second reference outputs a pulse the presence of which indicates an edge having too large an amplitude, most likely resulting from a noise pulse or a data transition. This second set of comparators would then be used to inhibit or flag the output of the first set of comparators in order to prevent these invalid edges from being further processed.

One skilled in the art will recognize that the above described functions and components are somewhat more complex than represented by the present block diagrams, however from the disclosure and teachings herein, taken with the available applications literature available from the manufacturers of the suggested components, or from other components which may be substituted as will be known from the above disclosure, the construction of a practical and operable device will be well within the capability of one or ordinary skill in the art without resorting to further invention or undue experimentation.

FIG. **21** is a flow chart of a synchronizing signal identifying method in accordance with the present invention. The video type signal is first received, followed by the detection of a first event and the detection of a second event. The relationship between the first and second event is determined and if the relationship matches known parameters the occurrence of the sync is identified.

It will be understood that the previous descriptions and explanations are given by way of example, and that numerous changes in the combinations of elements and functions as well as changes in design of the above may be made without departing from the spirit and scope of the invention as hereinafter claimed. In particular, will be useful to combine the functions of the invention with other functions in a fashion so that such functions may be shared between devices or methods. These and other modification to and variations upon the embodiments described above are provided for by the present invention, the scope of which is limited only by the following claims.

What is claimed is:

1. A processing apparatus, implemented in analog or digital form or both, for recovering synchronizing information from a video type signal including:

circuitry responsive to said video type signal to provide a first reference taking signal which is responsive to and occurs after a falling sync edge and to further provide at least a second reference taking signal which is responsive to and occurs after a rising sync edge;

circuitry responsive to synchronizing pulses of said video type signal and said first and second reference taking signals to generate at least a first reference level signal in response to said first reference taking signal and a second reference level signal in response to said second reference taking signal, said reference level signals representing different levels of said synchronizing pulses; and

circuitry responsive to said synchronizing pulses of said video type signal and a level responding to said reference level signals to generate recovered synchronizing pulses.

2. An apparatus, in analog or digital form or both, for recovering synchronizing information from a video type signal including:

clamping circuitry responsive to said video type signal to provide a clamped signal;

circuitry responsive to said clamped signal to provide a plurality of reference taking signals;

circuitry responsive to synchronizing pulses of said video type signal and said plurality of reference taking signals to generate at least a first reference level signal and a second reference level signal, said reference level signals representing different levels of said synchronizing pulses; and

circuitry responsive to said synchronizing pulses and a level responding to said reference level signals to generate recovered synchronizing pulses, with said reference taking signals being independent of said level responding to said reference level signals.

3. A video type signal processing apparatus, in analog or digital form or both, for producing logic level sync pulses including:

circuitry for generating a plurality of sampling signals each of which is responsive to an edge of a sync pulse of said video type signal and is delayed with respect to said edge;

circuitry for taking samples of synchronizing pulses of said video type signal and for providing samples of synchronizing pulse levels in response to said plurality of sampling signals, said circuitry for taking samples operable to generate at least a first reference level signal and a second reference level signal, said reference level signals respectively representing said synchronizing pulse levels, and with said sampling signals being independent of said reference level signals; and

comparing circuitry operable to compare said synchronizing pulses of said video type signal with a level responding to said reference level signals to generate said logic level sync pulses.

4. A video type signal processing apparatus, implemented in analog or digital form or both, for producing logic level sync pulses including:

clamping circuitry responsive to said video type signal to provide a clamped signal;

circuitry for generating a plurality of sampling signals each of which is responsive to an edge of a sync pulse of said clamped signal and is delayed with respect to said edge;

circuitry for taking samples of synchronizing pulse of said video type signal and for providing samples of synchronizing pulse levels in response to said plurality of sampling signals, said circuitry for taking samples operable to generate at least a first reference level signal and a second reference level signal, said reference level signals respectively representing said synchronizing pulse levels, and with said sampling signals being independent of said reference level signals; and

comparing circuitry operable to compare said sync pulses of said video type signal with a level responding to said reference level signals to generate said logic level sync pulses.

5. A video signal processing apparatus, implemented in analog or digital form or both, for use with a video signal having synchronizing pulses including horizontal synchronizing pulses including:

circuitry responsive to said horizontal synchronizing pulses to provide a plurality of reference taking signals;

circuitry responsive to said horizontal synchronizing pulses and said plurality of reference taking signals to provide at least a first reference level signal and a second reference level signal, said reference level signals respectively representing different levels of said horizontal synchronizing pulses; and

circuitry for comparing said synchronizing pulses of said video signal with a level responding to said reference level signals to generate logic level pulse versions of said synchronizing pulses, with said reference taking signals being independent of said level responding to said reference level signals.

6. A video type signal processing apparatus, implemented in analog or digital form or both, for producing logic level sync pulses including:

circuitry for generating a plurality of sampling signals;

circuitry for sampling horizontal synchronizing pulses of said video type signal in response to said plurality of sampling signals, said circuitry for sampling operable to generate at least a first reference level signal and a second reference level signal, said reference level signals respectively representing different levels of said horizontal synchronizing pulses; and

comparing circuitry operable to compare said horizontal synchronizing pulses of said video type signal with a level responding to said reference level signals to generate said logic level sync pulses with said sampling signals being independent of said level responding to said reference level signals.

7. A method for processing a sync portion of a video type signal, said sync portion having a plurality of levels, comprising steps of:

a) a first separation of said sync portion to generate a first separated sync signal;

b) generating a plurality of level signals each being representative of a level of said sync portion, at least one of which level signals is also generated in response to an edge of said first separated sync signal and is delayed at least 0.1 μs with respect thereto;

c) providing a reference signal in response to said plurality of level signals;

d) a second separation of said sync portion in response to said reference signal to provide a second separated sync signal which is a version of said sync portion.

8. A method as claimed in claim **7** where in said step b) includes holding one level of said sync portion at a known value in response to said first separated sync signal, and with step d) performed on said sync portion having one level held.

9. A method of detecting a sync pattern in a video type signal including the steps of:

a) detecting the occurrence of a known first event and generating a marking signal in response thereto;

b) delaying said marking signal by an amount which will provide a delayed version thereof before the expected occurrence of a known second event;

c) detecting an edge of said second event of transition from one state to another;

d) comparing said delayed version of said marking signal and said second event to ensure a proper relationship thereof.

10. The method as claimed in claim **9** including the inspection of a third transition event occurring in said sync pattern relative to said first event to ensure a proper relationship thereto.

11. The method as claimed in claim **9** including the inspection of a third transition event occurring in said sync pattern relative to said second event to ensure a proper relationship thereto.

12. A method of detecting a sync pattern in a video type signal including the steps of:

a) detecting the occurrence of a transition of a known direction and at least a minimum amplitude and generating a marking signal in response thereto;

b) delaying said marking signal by an amount which will provided a delayed version thereof at or before the expected occurrence of a known second event;

c) detecting said second event which includes an edge of transition from one state to another;

d) comparing said delayed version of said marking signal and said second event to ensure a proper relationship thereof.

13. The method of detecting a sync pattern in a video type signal including the steps of:

a) detecting the occurrence of a level of a component of said sync pattern for a known amount and time and generating a marking signal in response thereto;

b) delaying said marking signal by an amount which will provide a delayed version thereof at or before the expected occurrence of a known second event;

c) detecting said second event which includes an edge of transition from one state to another;

d) comparing said delayed version of said marking signal and said second event to ensure a proper relationship thereof.

14. A method for detecting an occurrence of a sync signal of a known pattern including the steps of:

a) detecting a first transition of a known direction and amplitude;

b) delaying an indication of the occurrence of said first transition for a known amount of time;

c) detecting a second transition of a known direction and amplitude;

d) detecting the approximate coincidence of said delayed indication and said second transition.

15. A method for detecting an occurrence of a sync event of a known pattern including the steps of:

a) detecting a first transition of a known direction and amplitude;

b) delaying an indication of the occurrence of said first transition for a known amount of time;

c) detecting a second transition of a known direction and amplitude;

d) detecting the approximate coincidence of said delayed indication and said second transition;

e) checking if said first or second occurrence takes place in an expected relationship to a previous event.

16. A method for detecting an occurrence of a sync event of a known pattern including the steps of:

a) detecting a first transition of a known direction and amplitude;

b) delaying an indication of the occurrence of said first transition for a known amount of time;

c) detecting a second transition of a known direction and amplitude;

d) detecting the approximate coincidence of said delayed indication and said second transition;

e) checking if said first or second occurrence takes place in an expected relationship to a later event.

17. The invention of claim 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14, 15 or 16 wherein data reference signals are generated in response to levels of said sync.

18. The invention of claim 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14, 15 or 16 wherein data reference signals are generated in response to levels of said sync, and in further response to data of said video type signal.

19. An analog, digital or combination apparatus for detecting a sync portion of a video type signal including:

a) circuit for detecting the occurrence of a known polarity transition of a known first event of said sync portion and generating a marking signal in response thereto;

b) delay circuit responsive to said marking signal to provide a wider marking signal before the expected occurrence of a known second event;

c) circuit for detecting said second event defined at least by a known polarity transition of said sync portion defining said second event;

d) circuit for comparing said wider marking signal and said second event to ensure a proper relationship thereof.

20. The apparatus as claimed in claim 19 further including a circuit for inspecting a third transition event of said sync portion relative to said first event to ensure a proper relationship thereto.

21. The apparatus as claimed in claim 19 further including a circuit for inspecting a third transition event of said sync portion relative to said second event to ensure a proper relationship thereto.

22. The method of identifying the occurrence of a sync event in a video type signal including the steps of:

receiving said video type signal;

detecting a known first event in said video type signal;

detecting a known second event in said video type signal;

detecting a known third event in said video type signal;

determining the relationship of said first and said second and said third events, and

should said relationship match known parameters identify the occurrence of said sync event.

23. A method for detecting in a video type signal an occurrence of a sync portion having a sync tip and a back porch, including the steps of:

a) clamping said video type signal with a sync tip clamp to provide a clamped signal;

b) low pass filtering said clamped signal to provide a filtered signal;

c) measuring the level of one of said sync tip or said back porch during the time period starting at least 0.1 microsecond after the start of said sync tip or reference level and ending before the end of said sync tip or reference level;

d) in response to said level of c) generating a 50% level signal representative of the midpoint between said sync tip and said back porch;

e) comparing said filtered signal and said 50% level signal to generate a logic level sync signal which is a version of said sync signal;

f) in response to a previous logic level sync signal from step e), generating a window signal representative of the expected occurance of a current logic level sync signal;

g) comparing said window signal to said logic level sync signal output of step e) and passing said logic level sync signal if it occurs within said window signal and blocking said logic level sync signal otherwise.

24. A method as claimed in claim 23 further including:

h) in response to said logic level sync signal of g) providing a horizontal signal having a duration of approximately one half horizontal period;

i) in response to said logic level sync signal of g) providing a vertical sync signal thereof;

j) comparing said horizontal sync signal of h) with the leading edge of said vertical sync signal of i) to generate a signal indicating odd and even fields, which signal changes polarity at the leading edge of said vertical sync signal.

25. An apparatus for detecting in a video type signal the occurrence of a 2 level sync portion having a sync tip and a reference portion, including:

a) circuitry for detecting the presence of a pattern of values representing said sync portion and operative to generate a first signal in response to the occurance thereof, said pattern including said reference portion followed by said sync tip for a known duration followed by said reference portion;

b) a delaying circuit for generating a delayed signal a delay period after said first signal, said delay period being the period until the next expected occurance of said pattern of values as detected by a);

c) a coincidence circuit responsive to the coincidence of said delayed signal and said next occurance of said pattern of values and operative to generate an output signal, which output signal signifies the occurrence of said sync portion, said coincidence circuit further operative to couple said output signal to said delaying circuit b).

26. An apparatus as claimed in claim **25** wherein said video type signal includes digital data which is represented by multiple data levels said apparatus further including:

d) level detecting circuit responsive to said video type signal to determine the level of said sync tip and said reference portion;

e) reference level circuit responsive to said level of sync tip and said reference portion in d) to generate a plurality of data slicing levels;

f) comparison circuit responsive to said video type signal and said plurality of data slicing levels to identify which said data level said video type signal falls into at known times.

27. An apparatus as claimed in claim **26** wherein said level detecting circuit of d) is further responsive to determine the levels of a plurality of said sync tip and a plurality of said reference portion, and said reference level circuit of e) is responsive to d) to change said data slicing levels between successive ones of said sync portions in response to changes in the levels of said sync tip and said reference portion.

28. A method for processing a data portion of a video type signal which includes a sync pulse, said sync pulse having a plurality of levels including a first level which is lower than the highest data level and a second level which is higher than the lowest data level, comprising steps of:

a) determining the value of said first level;

b) determining the value of said second level;

c) establishing an upper data reference level in response to the value of a);

d) establishing a lower data reference level in response to the value of b);

e) generating a plurality of data slice levels in response to the levels of c) and d);

f) comparing said data portion to said data slice levels of e) to determine which data level said data portion occupies at given instances.

29. The method as claimed in claim **14**, **15** or **16** wherein said known amplitude of a) is determined by requiring the amplitude of said first transition to be greater than a minimum value.

30. The method as claimed in claim **14**, **15** or **16** wherein said known amplitude of a) is determined by requiring the amplitude of said first transition to be greater than a minimum value and less than a maximum value.

31. The method as claimed in claim **14**, **15** or **16** wherein said known amplitude of c) is determined by requiring the amplitude of said second transition to be greater than a minimum value.

32. The method as claimed in claim **14**, **15** or **16** wherein said known amplitude of c) is determined by requiring the amplitude of said second transition to be greater than a minimum value and less than a maximum value.

33. The method of recovering sync from a video type signal including the steps of:

a) coupling said video type signal through a capacitor or other circuit thereby establishing a level shifted signal having a sync portion;

b) comparing said level shifted signal to a first known reference to provide a compared signal;

c) selectively adding a current to said level shifted signal wherein the amount and/or polarity of said current is responsive to said compared signal and the D.C. level of said level shifted signal is changed in response to said current;

d) comparing said level shifted signal to a second known reference to provide a second compared signal, which second compared signal is a logic level representation of said sync portion.

34. The method as recited in claim **33** wherein in step c) said sync portion is clamped to a known D.C. level thus providing sync tip clamping of said level shifted signal.

35. The method as recited in claim **33** wherein in step c) a first substantially constant current is taken from said level shifted signal and a second current is added to said level shifted signal through a diode in response to said compared signal being at a known level, said step c) thereby clamping the tip of said sync portion to a known D.C. level.

36. The method as recited in claim **33**, **34** or **35** wherein in step d) said second known reference is established at substantially the 50% level of said sync portion.

37. The method as recited in claim **33**, **34** or **35** wherein step d) includes measuring at least one of the highest or lowest level of said sync portion as part of establishing said second known reference.

38. The method as recited in claim **33**, **34** or **35** wherein step d) includes measuring the highest and lowest level of said sync portion as part of establishing said second known reference.

39. The method as recited in claim **33**, **34** or **35** including the further steps:

e) in response to said second compared signal of d), generating an adjustable window signal;

f) comparing said second compared signal of d) to said window signal and selectively passing or blocking said second compared signal in response thereto;

g) adjusting said window signal of e) in response to the expected format of said video type signal.

40. The method of detecting a sync segment of a video type signal which may be an HDTV signal including the steps of:

a) responding to sync pulses by inspecting said video type signal for the occurrence of a first transition in a known direction between a plurality of levels of known amounts followed at a known time by a second transition in a known direction between said plurality of levels and providing a sync signal in response thereto;

b) delaying said sync signal for a period corresponding to the expected period until the next arriving one of said sync pulses satisfying step a) thereby providing a delayed sync signal;

c) inspecting said delayed sync signal of step b) and a next arriving sync signal from step a) and in response to the substantial coincidence thereof providing a segment signal indicating the arrival of said sync segment.

41. The method of providing an output segment signal indicating the presence of sync segments of a video type signal which may be an HDTV signal including the steps of:

a) delaying said output segment signal for a period corresponding to the expected period between said sync segments, thereby providing a delayed signal having delayed indications of said sync segments;

b) inspecting said video type signal for the occurrence of a first transition in a known direction between a plurality of known levels followed a known time later by a second transition in a known direction between said plurality of levels and providing a sync signal having current indications of each said occurrence;

c) responding to said delayed signal of step a) and said sync signal of step b) in response to the coincidence of said delayed indication and said current indication to provide said output segment signal.

42. The method of claim **41** including the additional steps of;

d) detecting the loss of said delayed or current indications;

e) altering step c) to provide said output segment signal upon occurrence of said sync signal of b) without consideration of said coincidence.

43. The method of claim **41** including the additional steps of;

d) detecting a latch up condition in step c said condition preventing said coincidence;

e) altering step c) to provide said output segment signal upon occurrence of said sync signal of b).

44. The method as claimed in claim **40**, **41**, **42** or **43** including the further steps of:

f) sampling said video type signal after said first transition and before said second transition;

g) in response to step f), establishing a plurality of threshold levels;

h) periodically outputting a digital number representative of the amplitude of said video signal with respect to said threshold levels.

45. The method as claimed in claim **40**, **41**, **42** or **43** including the further steps of:

f) sampling said video type signal after said first transition and before said second transition;

g) sampling said video type signal either before said first transition or after said second transition;

h) in response to steps f) and g), establishing a plurality of threshold levels;

i) inspecting said video signal with respect to said plurality of threshold levels of step h) and periodically outputting a digital number representative of the amplitude of said video signal with respect to said threshold levels.

* * * * *

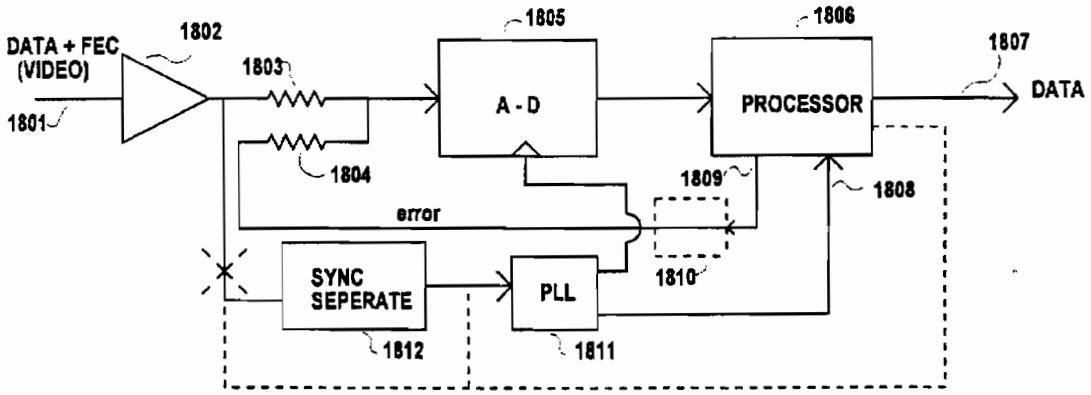

FIGURE 18

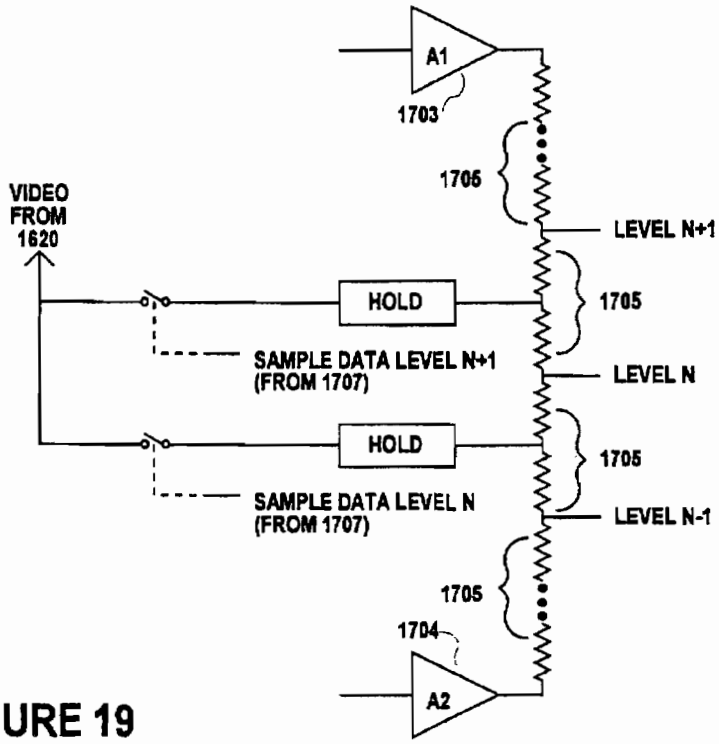

FIGURE 19

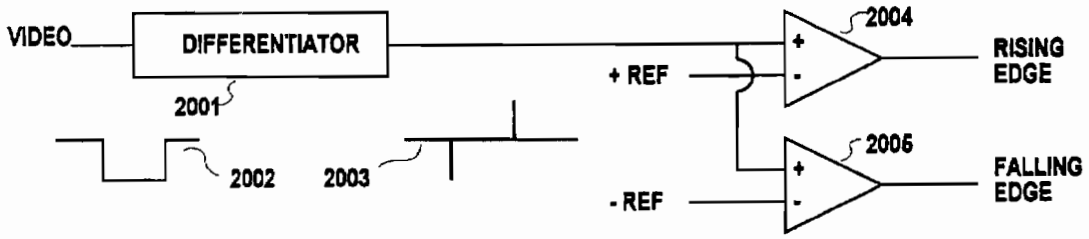

FIGURE 20

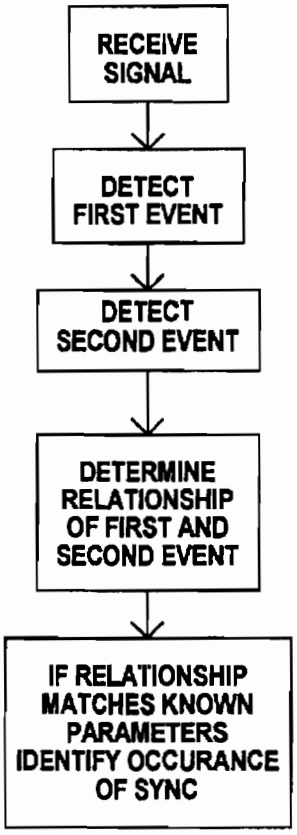

FIGURE 21

SYNCHRONIZING SIGNAL SEPARATING APPARATUS AND METHOD

This application is a continuation-in-part of application Ser. No. 08/493,661, filed Jun. 22, 1995, now abandoned which is a continuation in part of U.S. patent application Ser. No. 08/165,688 filed Dec. 13, 1993 now U.S. Pat. No. 5,486,869.

BACKGROUND OF THE INVENTION

The present invention relates to signal processing systems and, in particularly, to video signal processing. A major objective of the present invention is a synchronizing signal processing apparatus and a method that precisely recovers synchronizing signals of a video signal.

Much of modern technology depends on signal processing. A common application of signal processing is for the video type signals. Usually, a video type signal includes an information signal component and picture or data synchronizing information comprised. The synchronizing information is transmitted for scanning in a receiver in exact synchronism with a camera-tube scanning. The synchronizing signal must first be recovered from the video signal.

More particularly, TV (Television) video signals, the example of the video signal, are processed to obtain desired picture quality. A TV transmitting station modulates video and audio signal component and a synchronizing component which is used to identify the location of segments of the information component. The synchronizing component typically is comprised of a predetermined sequence of characteristics which are repeated periodically. Most commonly, NTSC television signals are comprised of an active video portion with two level sync pulses periodically positioned between the active video portions. In particular, in order to precisely reproduce pictures, synchronizing information is added in the video signal so that the receivers can synchronously perform scanning operation as the TV transmitting station does.

Numerical and graphical criteria which describe essential aspects of a TV system, employed in the design and operation of equipment to assure that the various parts of the system will operate in cooperative fashion at maximum performance. TV systems have a special need, compared with other communication systems, for definitive standards because television transmitters and receivers must operate in a precise lock-and-key relationship. In particular, the scanning of the image in the camera must be matched by the scanning in every associated receiver within a timing precision of approximately one-tenth of a millionth of a second, and with relative positions of picture details correct to a few hundredths of an inch as viewed on the CRT or other display.

To assure that any television receiver can receive programs from any transmitter within range, it is customary to set up a single set of standards with a group of neighboring countries. The TV transmitting stations of different countries and areas transmit video signals with different formats. For example, U.S.A., Canada and Japan et al. use NTSC (National Television System Committee) system. France, the former Soviet Union countries et. al. use SECAM. Moreover, HDTV (High Definition TV) creates a new system with images of high resolution as well as a new video signal format and new transmission methods. For all of these examples, the synchronizing signals added in their video signals are different, but share similar characteristics.

Picture synchronizing information is obtained from the video signal by means of sync separation circuits. In addition, these circuits must separate this information from noise and interference during the reception of weak signals, particularly if impulse noise is present. To reproduce these different video signals of respective systems, different video signal processing devices are needed to provide required synchronizing signals.

Conventional video signal devices for processing the synchronizing information of the video signals can not be used for different standard video signals for providing reliable synchronizing signals, without affecting the reproduction of the video signals or causing high cost of video signal processing. What is needed is a synchronizing signal processing apparatus and method that precisely recovers synchronizing signals of the video signal and can be applied for processing different video signals.

SUMMARY OF THE INVENTION

The present invention provides for detecting a synchronizing portion of a video type signal, and for signals which transmit digital or constrained multilevel analog data providing reference signals fro slicing the data portion of the signal in response to the synchronizing component. As used herein for the purposes of describing and claiming the present invention the video type signal will be described as the type having periodic known patterns which comprise the sync portion with the sync portions being interspersed with video like or other information carrying signals such as data with this information carrying portion being referred to as video and data both terms of which are intended to include any information carrying signal. A group consisting of at least a sync portion and a information carrying portion will be referred to as a data group.

This process of detecting the synchronizing portion of the video type signal involves identifying or detecting the arrangement of the known pattern of the sync or other identifier. For purposes of describing and claiming the present invention detecting shall be understood to encompass, inspecting, identifying, recognizing, distinguishing and any other means or method of ascertaining the presence, occurrence or location of the feature of interest. The present invention provides for such detecting by detecting a first transition of a known direction and amplitude, and inspecting the first transition to see if it occurs in a proper relation to a second known occurrence. The detection of the proper relation of the known occurrences is preferred to be made by delaying a signal marking the first occurrence for an amount equal to the expected arrival of the second occurrence and determining if the two are approximately coincident, thereby indicating the proper relationship. Further checking may be made by including a third or more occurrences to ensure proper relationships, for example by checking to determine if the first or second occurrence takes place an expected time before or after an event.

In order to establish references for data slicing the amplitude and D.C. level of components of the sync portion are used to establish the D.C. level and gain of the reference signals. Because the gain and D.C. levels may change throughout the signal, it becomes necessary to remove these changes from the signal and/or adjust the references accordingly. This capability is provided by establishing or measuring some known parameter at each end of a segment of data or video in order to be able to estimate these changes, or eliminate these changes, during the segment.

In accordance with the present invention, a synchronizing signal processing apparatus includes means for sampling synchronizing type signals and components of a video type

signal. The present invention further includes slicing a video type signal in response to the sampled synchronizing signals. The synchronizing signal processing apparatus includes a sampling means that samples synchronizing signal components and provides at least a reference signal. The synchronizing signal processing apparatus also includes a comparing means that slices the video signal in response to at least a reference signal responsive to different levels of components of the synchronizing pulses. Thus, the synchronizing signal processing apparatus generates logic level outputs. The video signal with which the present invention is used may be of a standard type having synchronizing pulses including horizontal synchronizing pulses or may be of the proposed HDTV type or of other type having a sync portion made up of a known sequence of components and a information carrying portion carried therewith.

The video signal may be sliced, before it is sampled, to eliminate noise. The sliced video signal corresponds to the synchronizing pulses. In response to the sliced video signal, the peaks of the synchronizing pulses of the video signal are precisely sampled. Two sampled signals represent the positive and negative peaks of the synchronizing pulses. The two sampled signals further are divided into three reference signals to compare with the video signal. After this comparison, the logic outputs are combined to recover synchronizing pulses that are reliable, precise and without noise.

A combining means couples to the comparing means so that the outputs from the comparing means are combined depending on the type of the video signal. The combining means generates a plurality of synchronizing signals.

To provide a vertical synchronizing signal, the present invention uses an integrating type filtering means that filters one of synchronizing signals output from the combining to provide a vertical synchronizing signal. The filter means shows a good frequency response characteristic for the vertical synchronizing signal.

The synchronizing signal processing method in accordance with the present invention comprises steps of slicing a video signal, sampling the video signal in response to respective leading and trailing edges of the sliced signal, converting the sampled signal into at least a reference signal, comparing the reference signal with the video signals and combining the compared outputs to recover synchronizing pulses.

An advantage of the synchronizing signal processing apparatus and method is that the present invention incorporates several standard functions with superior performance. The synchronizing signal processing apparatus in accordance with the present invention is capable of operating with standard two level synchronizing pulses, for example, NTSC, PAL and SECAM type synchronizing pulses, and three level synchronizing pulses, for example HDTV synchronizing pulses. The present invention may also applied for other video type signals with synchronizing pulses.

Furthermore, the present invention provides good bandwidth properties and time constant in the video amplifier section. The combination of both proper bandwidth and time constant gives considerably noise immunity against high frequency noise, yet maintains sufficient operation speed for high performance. Therefore, no additional compensation or filtering components are needed.

The synchronizing signal processing apparatus in accordance with the present invention may be easily adjusted for either two level or three level synchronizing pulses. The recovered synchronizing levels for video signals are characterized by high precision and reliability.

The logic level outputs of the comparing means are combined, the combination depending on whether the synchronizing pulses are two levels or three levels. In accordance with the present invention, the synchronizing signal processing apparatus may generate a TTL (Transistor-Transistor level) version of the synchronizing pulses.

The synchronizing signal processing apparatus in accordance with the present invention may be used with different video devices, which simplifies the design and manufacture of video devices, and significantly decreases the cost to make these video devices.

Another advantage of the synchronizing signal processing apparatus of the present invention is that it is suitable to be implemented by integrated circuits. Alternatively, the video signal processing can be implemented by software, such as in signal processing applications. These and other features and advantages of the present invention are apparent from the description below with reference to the following drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. **1** is a block diagram of a synchronizing signal processing apparatus in accordance with the present invention.

FIG. **2** illustrates a detailed circuit diagram of a sync pulse processing section of the synchronizing signal processing apparatus of FIG. **1**.

FIG. **3** illustrates a detailed circuit diagram including a pulse width adjust and a reference sync generating section of the synchronizing signal processing apparatus of FIG. **1**.

FIG. **4** illustrates a detailed circuit diagram of a sync restoring section of the synchronizing signal processing apparatus of FIG. **1**.

FIG. **5** shows waveform diagrams of several nodes of the synchronizing signal processing apparatus.

FIG. **6** shows a frequency response characteristic of a filter device of the synchronizing processing apparatus of FIG. **1**.

FIG. **7** is a flow chart of a synchronizing signal processing method in accordance with the present invention.

FIGS. **8–11** are four sheets of a detailed schematic of the preferred embodiment in accordance with the present invention.

FIG. **12** shows a prior art HDTV video format waveform which has a two level sync pulse and an 8 level digital data format.

FIG. **13** shows a prior art HDTV video format which utilizes a two level sync pulse and a 16 level digital data format.

FIG. **14** shows an expanded diagram of a typical one of the syncs of FIG. **12** or **13**.

FIG. **15** shows a typical expanded diagram of a typical pair of single data segments separated by a single sync pulse.

FIG. **16** shows a diagram of the preferred embodiment of the present invention

FIG. **17** shows a diagram of the preferred embodiment of the present invention for providing thresholds and slicing data.

FIG. **18** shows a digital embodiment of the present invention.

FIG. **19** shows a diagram of the preferred embodiment of the present invention for providing thresholds in response to data.

FIG. **20** shows a diagram of the preferred embodiment of the present invention for detecting edges of known magnitude.

FIG. **21** is a flow chart of a synchronizing signal identifying method in accordance with the present invention.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

A synchronizing signal processing apparatus **100** in accordance with the present invention includes an input amplified **102**, a video standard detector **103**, a sync pulse processing section **104**, a pulse width adjust **106**, an offset device **108**, a DC (Direct Current) restoration device **110**, a reference sync generating section **112** and a sync restoring section **114**.

Video signal **116** is applied to differential input amplifier **102** where video signal **101** is amplified to improve the ratio of signal/common mode noise. The video signal amplified by input amplifier **102** is fed to sync pulse processing section **104** which includes a sync tip clamp **116**, a sync slicer **118** and a sync tip peak detector **120**.

The video signal is first clamped by sync tip clamp **116** to generate a clamped signal which has a known DC level of the synchronizing pulses. The clamped signal is then transferred to sync slicer **118** where the clamped signal is sliced, thereby generating a signal that has the same time period as that of the synchronizing pulses but at standard levels as compared to that of the synchronizing pulses, in this example TTL levels. To effectively eliminate interference and noise, the sync slicer **118** slices the synchronizing pulses at a known level which is preferred to be about half of the nominal expected amplitude of the synchronizing pulses. Due to a known level which is approximately half the expected level, the operation of sync slicer **118** may be considered a coarse slicing operation which provides coarse sliced pulses. The sliced signal is coupled to sync tip peak detector **120**, in which peaks of synchronizing pulses of the video signal from DC restoration device **110** are sampled in response to the sliced signal.

The clamped signal is also delivered to pulse width adjust **106**. This clamped signal activates pulse width adjust **106** to generate a pulse trigger signal coupling to DC restoration device **110**. The pulse trigger signal determines the pulse width of the synchronizing pulses. A switch SW_P is provided so that this switch is open, which indicates that the video signal is a NTSC TV signal. On the other hand, when the video signal output from the input amplifier **102** is a HDTV signal, the video standard detector **103** will turn switch SW_P on. The video standard detector **103** also control switches SW_T, SW_U, and SW_L. The switches may be operated automatically in response to a video standard detector **103** which detects the type of signal **101**. Therefore, the synchronizing signal processing apparatus **100** in accordance with the present invention may process different video signals.

Offset device **108** provides a DC reference for DC restoration **110**. The amplified video signal from the input amplifier **102** is also coupled to DC restoration **110**. In response to the reference from offset device **108**, DC restoration **110** clamps the amplified video signal to eliminate DC shift and residual common mode noise.

Other types of DC restoration circuits may be used as is well known in the art. It is desired to have the video signal $V0_1$ and $V0_2$ restored to a known value. However, it should be noted that the DC restoration device **110** may be eliminated by directly AC coupling the video signal output from the input amplifier **102** to the reference sync generating section **112** and sync pulse processing section **104**. The operation of sync tip peak detector **120** will track the variations in the AC coupled video signal output from the input amplifier **102** and allow the comparator **122** to function properly. However, the use of a DC restoration device is preferred. The DC restoration device **110** produces two output signals $V0_1$ and $V0_2$. The clamped video signal $V0_2$ is delivered to sync tip peak detector **120**. In response to the sliced signal from the sync slicer **118**, sync tip peak detector **120** samples the positive and negative peaks of synchronizing pulses of the clamped video signal so as to provide two peak sample pulse signals. For purpose of the present example, video is described with respect to positive white with the negative level of sync being that which is farthest from peak white video and the positive level of sync being that which is closest to the peak white value of the video. For two level sync, such as NTSC, the positive peak will correspond to video blanking level. The two peak sample pulse signals define each of synchronizing pulse. Divider **124** receives them and converts them into three pulse reference signals. The amplitudes of the pulse reference signals represent percentage levels of sync of $V0_2$ during the respective ones of the peak sample pulses as represented by V_H and V_I.

Reference sync generating section **112** also includes a comparator **122**. The clamped video signal from D.C. restoration **110** and three pulse reference signals are coupled to comparator **122**. By comparison, comparator **122** outputs four level signals during each synchronizing pulse of the video signal. Due to the use of references which are responsive to the actual level of the sync pulse, the comparator **122** may be considered a precision comparator, which outputs precision sliced pulses. The four level signals represent different amplitudes of each synchronizing pulse as determined by the video sync being greater than none, one, two or three of the pulse reference signals.

A sync restoring section **114**, which includes combination logic **126** and vertical sync filter **128**, is arranged to receive the output signals from the comparator **122** of reference sync generating section **112**. The combination logic **126** is used to combine the four output signals from comparator **122** to recover reliable synchronizing signals. Switches SW_U and SW_L are arranged to control the switching between the HDTV video signal and conventional TV video signals, for example NTSC TV video signal.

The opening of switches SW_U and SW_L indicates that the synchronizing signal processing apparatus operates with conventional video signal. Otherwise, the closing of the switches SW_U and SW_L shows out that the apparatus operates with HDTV video signal. The position of another switch SW_T is also related to the video signal being processed by the apparatus in according with the present invention. Therefore, the apparatus of the present invention is suitable to different video signals by changing status of these switches, which may respond automatically to the video standard detector **103** as well.

The vertical sync filter **128** is coupled to the combination logic **126**. A composite synchronizing signal C_S from the combination logic **126** is coupled to it. The vertical sync filter **128** filters the composite synchronizing signal C_S to provide a vertical synchronizing signal V_S. The vertical sync filter **128** may respond to composite synchronizing signal from other sections as well, for example from **112**.

The sync pulse processing section **104** of synchronizing signal processing apparatus **100** is detailed with reference to FIG. **2**. Input amplifier **102** includes two operational amplifiers OP1 and OP2. OP1 is used with OP2 to eliminate common mode noise of the video signal **101**. The positive input of OP1 receives one of input video signal **101** which is the common one (shield) of the input signals. Resistor R1,

100KΩ, is an input resistor for stabilizing the DC component of the input video signal.

A resistor R2 (75Ω) and a switch SW_I are connected between the input lines for terminating video signal **101**. When the input is taken from other than the end of a coaxial cable run, SW_I is open. While the video signal **101** is applied to input amplifier **102** at the end of a coaxial cable run, SW_I is closed so that the input resistance of input amplifier **102** is matching the output resistance of the circuitry providing video signal **101**, thereby reducing signal loss. Capacitor C1 (0.1 μf) provides a high frequency bypass from the common to ground. R2 is the terminating resistor (75Ω). OP1 and resistors R3 (1.10KΩ) and R4 (499Ω) constitute a negative feedback amplifier its gain being two approximately. The output of OP1 is coupled to the negative input of OP2 via resistor R5 (2.21KΩ).

The positive input of OP2 receives the signal directly from the input signal **102**. OP2 and resistors R6, R7 and potentiometer R8 provide another feedback amplifier. Resistor R6 and R7 have the same resistance, 1.0KΩ. The potentiometer R8 has a resistance from 0–10KΩ. Thus, the gain of the input amplifier **102** may be adjusted between 1.5–3. Due to the delay caused by OP1, the common mode component of signal **102** arrives at the positive and negative inputs of OP2 at slightly different moment. Under low frequency, the delay due to OP1 is tolerable. However, high frequency components of the input video signal, after delay by OP1, would severely affect correlation of the common mode signal, causing distortion of video signal. Therefore, a filter having capacitor C1 of 0.01 μf is utilized to filter the interference and noise to ground.

The output of OP2 is coupled to the sync tip clamp **116** of the sync pulse processing section **104**. The sync tip clamp **116** includes buffers OP3 and OP4, and an amplifier OP5. Resistor R9 (5.6KΩ) is used with capacitor C2 to by-pass undesired frequency components. The buffered video signal is coupled to the positive input of another buffer OP4 via an isolating capacitor C3, 0.1 μf.

A negative 12V is applied to the isolating capacitor C3 and the positive input of OP4, via a current limit resistor R10, 147KΩ. R10 effectively constitutes a constant current source. The isolating capacitor C3 is used to isolate the direct current components of the video signal.

The negative 12V applied to the capacitor C3 draws node N1 toward a negative level, pulling the video signal output from OP3 to a negative level. The negative video signal, after buffering by buffer OP4, is coupled to the negative input of the amplifier OP5 via a resistor R11 with resistance of 10KΩ. OP5 and a resistor R12 with resistance of 39KΩ established a negative feedback amplifier. The positive input of OP5 is grounded. The resistance of the resistor R12 determines the maximum gain of amplifier OP5, which my be lowered if D3, D4 conduct.

Normally, the output of OP5 is negative. Two diodes D1 and D2 are provided to isolate the output of OP5 from the node N1. When the output of OP5 is above a level required to turn the D1 and D2 on, for example 1.2V, the capacitor C3 is charged positive. The resistor R10 charges C3 negative, but is countered by the current through D1 and D2 when the video signal is below the ground of the positive input of OP5, thus causing N1 to move in a positive direction, which forces the output signal of OP5 to be returned to a negative value. The other two diodes D3 and D4 are arranged between the negative input and output of OP5. When the video signal at the negative input of OP5 is more positive by a level high enough to turn D3 and D4 on, the negative input and output of OP5 are shorted so that OP5 functions as a buffer and prevents large negative excursions at the output, thereby causing OP5 to recover to normal status very quickly, when returning positive.

Sync slicer **118** includes a comparator CP6. The output of OP5 is directed to the positive input of CP6. The output of OP4 is directed to the negative input of CP6. By comparison of the signals at its inputs, CP6 slices the synchronizing pulses of the video signal at about half of the amplitude. By using both the outputs of OP4 and OP5, the comparison is less sensitive to noise and sync amplitude variations than if a fixed level were used. For the NTSC and HDTV video signals, the output of CP6 has a delay about 0.1 μS. Comparator CP6 slices the amplitude of the synchronizing pulses without appreciable change of pulse width.

The sliced pulses output from CP6 are directed to the sync tip peak detector **120**. The sync tip peak detector **120** includes sample switches SW_1 and SW_2, and two sample holders consisting resistors R15 and R16 with the same resistance of 1KΩ, and capacitors C6 and C7 with the same capacitance of 0.1 μf. Resistor R15, capacitor C6 and switch SW_1 constitute a sample and hold circuit. Resistor R16 and capacitor C7 and SW_2 constitute another sample and hold circuit. Two buffers OP7 and OP8 are respectively coupled to the two sample and hold circuits to output the sampled signals.

The sliced pulsed from CP6 are first inverted by an inverter I1. Thus, the rising edge of the inverted pulses coincide with the trailing edge of the output pulses of CP6. Each of the inverted pulses is then differentiated at its rising edges, by means of a differential capacitor C4 of 0.001 μf and a differential resistor R13 of 330Ω. The switch SW_1 is in the receipt of the signal $V0_2$ output from the DC restoration device **110**. Usually, switch SW_1 is tied to ground via resistor R13. Only upon the arrival of the rising edges of the inverted pulses, switch SW_1 is activated to couple to the hold circuit having R15 and C6. Therefore, corresponding to each falling edge of the sliced pulses output from CP6, R15 and C6 sample the positive peaks of the pulses. Note that the sliced sync from CP6 is opposite in polarity to the sync of $V0_2$. The sampled positive peak is held for the buffer OP7 to output. The width and amplitude of differential pulse for sampling the video signal is set by C4 and R13.

The sampling time may also be controlled by the addition of a oneshot in the path from the differential node N2 or N3 and the control input of the respective switch. It is preferred that the sampling start after all ringing which might be present on the preceding edge has had time to die out, or to an acceptable level, and end before any preshoot which may be present on the next edge, for the same reasons. It is also preferred that the sampling time be substantially equal to an integral number of cycles of any coherent or repetitive interference which may be present on the waveform in order that it will average or integrate to zero (if the interference is bipolar and uniformly distributed) or a steady value (if the interference is unipolar or nonuniformly distributed) in the hold circuit.

The amplitude of the pulse applied to the switch control input (or to the oneshot trigger input) is critical. It is desired to select the values of the differential network in relation to the expected amplitude and/or risetime of sync edges and to the switch control or oneshot input threshold to ensure that edges having less than the nominal value of sync edges (40 IRE units for NTSC) amplitude do not cause false sampling. Such low amplitude edges will sometimes occur in response to noise impulses which are so fast that the comparator CP6

is unable to make a full scale transition at its output during the pulse duration. The component values given in FIG. **9** provide such protection.

For example, for the ICs suggested the threshold is set internally at ½ VCC. The differentiation network should be designed so that a 35 IRE edge will result in a ½ VCC pulse which will cross the control threshold. This will guarantee that a proper 40 IRE edge will always generate a sample and a low 30 IRE noise edge will not generate a sample.

Similarly, after inversion twice by inverter **I2** and **I3**, the output of **CP6** is differentiated by a differential capacitor **C5** of 0.001 μf and a differential resistor **R14** of 330Ω. The delay of the inverter **I1–3** along with the delay of **116** ensures that the sample pulses are applied to SW_1 and SW_2 well after any ringing or other distortion on the sync or blanking level has died out. If desired, delay elements other than the inherent delay of the circuit elements may be introduced to further ensure proper sampling of the video. Thus a differential pulse is coupled to switch SW_2. The differential pulses produced by **C5** and **R14** cause the switch SW_2 close so that a resistor **R16** of 1KΩ and a capacitor **C7** of 0.1 μf hold the negative peaks of the synchronizing pulses. The two signals which operate sample switch SW_1 and SW_2 can be described as reference taking signals, since they take the instant samples which are in turn held by the hold capacitors to generate the voltage reference signals used by the divider **124** to provide references for comparator **122**.

As a result, each of the pair of differential pulses produced by **C4**, **R13**, **C5** and **R14** defines the pulse position of respective synchronizing pulses. The relationship of the output pulses of **CP6** and the differential pulses is shown in FIG. **5**. Furthermore, buffers **OP7** and **OP8** deliver the peak sample signals to divider **124** for further processing.

The video signal amplified by the input amplifier **102** is also coupled to the DC restoration device **110**, referring to FIG. **3**. The DC restoration device **110** includes a voltage comparator **CP9**, a photosensitive element having a LED (light-emitting diode) DU and a photoresistor **R59**, an amplifier **OP10** and buffer **OP11**. A positive 5V DC voltage is tied to a resistor **R17** of 1.0KΩ, the left part of the photoresistor **R59** and the top of **R59** is connected to ground. Thus, the voltage applied to the positive input of **CP9** depends on the resistance of the left part of **R59**. On the other hand, the positive 5V is tied to a series connection of potentiometer **R18** a resistor **R19** and to ground. Thus, the reference voltage at the negative input of **CP9** is defined by the position of the wiper of potentiometer **R18**. Therefore, adjusting the position of the wiper of potentiometer **R18** may change the input voltage at the negative input of **CP9**.

At the output of **CP9**, a positive 5V is applied to the LED D_u through a resistor **R20** of 200Ω. The positive 5V provides an offset current to LED D_u. The light intensity of the LED D_u is in proportion to the current flowing through it. The resistance of photoresistor **R59** is inversely proportional to the light intensity. Therefore, the higher the output of **CP9**, the larger the current through the LED D_u, the lower the resistance of the photoresistor **R59**. The lower resistance of **R59** makes the voltage applied to the positive input of **CP9** go down, thereby causing the output of **CP9** to decrease. **CP9** thus causes **R59** to maintain the voltage at the positive and negative inputs of **CP9** to be equal.

The output of the input amplifier **102** is coupled to the positive input of the amplifier **OP10** of DC restoration **110**, via a resistor **R2** of 330Ω. The output of **OP10** is tied to the negative input via a feedback resistor **R22**, 1.0KΩ and the right part of the photoresistor **R59** ties the negative input of **OP10** to ground. Because the output of **CP9** may change the resistance of **R59**, the gain of **OP10** is also controlled by the output of **CP9**. Therefore, changing the position of the wiper of potentiometer **R18** changes the gain of **OP10**. It will be understood from the present teachings that the same functions may be performed with other circuit elements, for example multipliers.

The output of **OP10** is applied to the positive input of amplifier **OP11**. Along with a resistor **R23** of 1.0KΩ, the operational amplifier **OP11** buffers the output of **OP10**. The video signal from buffer **OP11** is transferred to the sync tip peak detector **120** where the video signal is sampled in response to the pulses from the sync slicer **118**, as shown in FIG. **2**. The video signal output amplified by **OP10** is also sent out by an output resistor **R24**, 71.5Ω for other purposes.

An offset device **108** is arranged to provide a DC offset required by the operational amplified of the DC restoration **110**. The offset device **108** includes a resistor network having a resistor **R57** (100KΩ), a resistor **R55** (100KΩ) and a potentiometer **R55**. A positive 12V is coupled to resistor **R57** and a negative 12V is coupled to resistor **R56**. A voltage determined by the position of the wiper of potentiometer **R55** charges a capacitor of 0.1 μf via a resistor **R58** of 100KΩ. The level on the capacitor **C13** is applied to the positive input of a buffer **OP12**.

The offset voltage is delivered to an integrator circuit established by a operational amplifier **OP13** and a capacitor **C8** (0.1 μf) bridging between the negative input and output of **OP13**. The positive input of **OP13** receives the offset voltage. The offset voltage is also coupled to a switch SW_3. The common close status of SW_3 couples the offset voltage to the negative input of **OP13** via a resistor **R25** of 10KΩ. A capacitor **C9** of 0.001 μf is tied between ground and SW_3 for filtering undesired frequency components and switching transients.

In accordance with the present invention, the pulse width adjust **106** is provided for. The pulse width adjust **106** includes two multivibrators **301** and **302**. The output from the sync slicer **118** is coupled to the /A input of **301**, as shown in FIG. **3**. A positive 5V is tied to the clear input Clr of **301**. Responding to each falling edge of the sliced signal from sync slicer **118**, the multivibrator **301** produces a low level pulse at the Q output of **301**. The width of the low level pulse is set by a resistor **R54** of 10KΩ and a capacitor **C10** of 0.001 μf. The output from **301** is shown in FIG. **5**.

The output from sync slicer **118** is also coupled to the B input of multivibrator **302** via a delay circuit. This delay circuit includes two RC filters. A capacitor **C14** (51 pf) and a resistor **R28** (10KΩ) form a RC filter and a capacitor **C12** (56 pf) and a resistor **R60** (2.5KΩ) provide another one. Two inverters **I4** and **I5** are arranged between the two RC filters. An inverters **I6** is positioned between the B input of **302** and RC filter having **C12** and **R60**. A positive 5V is applied to **R28** via a resistor **R27** (1KΩ) for providing a DC bias. This delay circuit delays the sliced signal from sync slicer **118** about 0.75 μs to 0.9 μs.

The pulses at the /Q output of **301** trigger the multivibrator **302** via its /A input so that the Q output of **302** is at high level. The delayed pulses by the delay circuit is applied to B input of **302**, triggering it so that the Q output of **302** is at a high level. The pulse width of output pulse from **302** is set by a resistor **R29** of 3.32KΩ and a capacitor **C11** of 0.001 μf, if the apparatus **100** in accordance with the present invention operates under conventional TV video signal mode, for example, the NTSC video signal. When the

apparatus **100** operates under the HDTV mode, a resistor **R30** of 1KΩ is shunted with **R29** by closing of the switch SWP.

Therefore, the pulse width of Q output of **302** is between 2.0 μs and 2.5 μs for the NTSC video signal. This pulse occurs during blanking and burst portion of the NTSC video signal. On the other hand, the pulse width of the Q output of **302**, for the HDTV video signal, is from 0.5 μs to 0.7 μs. The pulse of Q output of **302** coincides with the blanking portion without exceeding it. The waveform at the Q output of **302** is shown in FIG. **5**.

The output pulses at the Q output of **302** activate the SW_3 so that the output from **OP11** is coupled to the negative input of **OP13** via the RC filter having the resistor **R25** and the capacitor **C9**. During the high level of the pulses from **302**, the capacitor **C8** of the integrator **OP13** is charged up and down by the video signal from the buffer **OP11** depending on whether it is above or below the reference on the plus input of **OP13**, drawing the input voltage at the positive input of **OP10** up or down. As a result, the output of **OP10** is drawn up or down. After the Q output of **302** recovers to low level, the switch SW_3 is released so that the negative input of the operational amplifier **OP13** is coupled to the output of **OP12** of the offset device **108**. Thus, the output of the operational amplifier **OP13** does not change.

The divider **124** of the reference sync generating section **112** includes four resistors **R31**, **R32**, **R33** and **R34**. The resistors **R31**–**R34** have the same resistance of 10KΩ. Therefore, the output potential of the sync tip peak detector **120** is equally divided so that three reference potentials are provided. The first reference potential between the resistors **R33** and **R34** equals half of the output potential from the sync tip peak detector **120**. The second reference potential between the resistors **R31** and **R33** equals three-fourth of the output level from the sync tip peak detector **120**. The third reference potential between the resistors **R32** and **R34** equals one-fourth of the output level from the sync tip peak detector **120**. However, different reference potentials may also be obtained by changing the resistance of resistors **R31**–**R34**. Different combination of potentials on the positive input of **CP14**–**CP16** can be easily realized.

In accordance with the present invention, the comparator **122** of reference sync generating section **112** includes three comparators **CP14**, **CP15** and **CP16**. The first reference potential between the resistors **R33** and **R34** is applied to the positive input of comparator **CP14**. The second reference potential between the resistors **R31** and **R33** is applied to the positive input of the comparator **CP15**. The third reference potential is then applied to the positive input of the comparator **CP16**. The video signal output $V0_1$ from the amplifier **OP10** of the DC restoration **110** is coupled to respective negative inputs of three comparators **CP14**–**CP16** via resistors **R35**, **R36** and **R37**.

As for conventional TV video signals, for example, the NTSC video signal, **CP14** compares the first reference potential and the video signal V_{01} so as to sense the middle levels of the horizontal and vertical synchronizing pulses. The comparator **CP15** then senses the video signal V_{01} in response to the second reference potential and the rest of the video signal V_{01} is regarded as noise. Because the switch SW_1 of sync tip peak detector **120** closes during the blanking-burst period to sample the video signal, the second reference potential is set to a level lower than the blanking level. The switch SW_2 of sync tip peak detector **120** closes during the negative synchronizing tip to sample the video signal, the third reference potential is thus set to a level higher than the negative tip. Two complementary output V_{P3} and V_{C3} from **CP16** are delivered to the combination logic **126**.

As a second example, when the apparatus **100** in accordance with the present invention is used for processing the HDTV video signal, the second reference potential represents a value between the blanking and positive peak synchronizing tip for the synchronizing pulses. The rest of the video signal V_{01} is considered as noise. The first reference potential is set at the middle of the negative and positive synchronizing tip during synchronizing pulses, meaning at the blanking level. The purpose of this comparator **CP14** is to sense transition from the negative synchronizing tip to the positive synchronizing tip. The rest of the video signal V_{01} is considered as noise. The reference potential and the output V_{P3} of **CP16** is the same as under the NTSC video signal. Therefore, outputs of comparator **122** are logic levels corresponding to the negative sync for these video signals.

The logic level outputs V_{P1}, V_{P2}, V_{P3} and V_{C3} from the comparator **122** are directed to the combination logic **126** of the sync restoring section **114**, as shown in FIG. **4**. The output V_{P1} of the comparator **CP14** is directed to an input of an AND gate A1. The signal V_{C3} output from the comparator **CP16** is inverted by an inverter **I7**, and is filtered by a RC filer having a resistor **R53** (200Ω) and a capacitor **C17** (0.001 μf). Before it is applied to another input of the AND gate A1, the filter signal V_{C3} is inverted again by an inverter **I8**. In order to preserve the combination logic generated sync information at the half way crossing, the output V_{C3} from the comparator **CP16** is delayed by the inverter **I7** and **I8** circuit for 85 ns–200 ns. Thus, the two input pulses are added at the inputs of the AND gate A1 so that the output of A1 is a positive pulse.

Along with the output from the AND gate A1, the output V_{P2} from the comparator **CP15** is directed to an input of an OR gate O1. The positive pulse from A1 and the V_{P2} activate the OR gate O1, thereby producing a pulse which has a rising edge defined by the positive pulse from A1 and a falling edge defined by V_{P2}. The output of OR gate O1 is directed to another OR gate O2.

The output V_{C3} is also used to trigger a multivibrator **401** so that a high level is set at the /Q output of the multivibrator **401**. The width of high level is set by a resistor **R38** and a capacitor **C18**. In this case of capacitor **C18** has a capacitance of 0.001 μf and resistor **R38** has a resistance of 2.9KΩ, the pulse width is between 1.4 μs–2.8 μs. The output high level at the /Q output of **401** is directed to an input of an AND gate A2. Another input of A2 receives the output V_{P3} from the comparator **CP16**. For the NTSC video signal, the output of A2 is determined by signal V_{P3}. Under the HDTV video signal, the output of A2 is determined by the pulse at the /Q output of **401**. The minimum width for this pulse is 2.6 μs which determined by the duration of the vertical interval pulses. The maximum width for this pulse is 2.8 μs which is determined by the duration of the blanking in horizontal lines.

The ANDed output from A2 is applied to another input of OR gate O2 so that the output from OR gate O1 is ORed with the ANDed output from A2. Particularly, under processing the NTSC video signal, the ORed output of OR gate O1 is completely determined by the ANDed output pulse from A2. The reason is that the negative ANDed output from A2 is narrower than the negative ORed output from O1. The output of O2 is a composite synchronizing output C_S.

In order to extract horizontal synchronizing pulses from the out C_S from the OR gate O2, a circuitry including

multivibrators **402** and **403**, and OR gates O3 and O4 is designed. This circuitry eliminates every second half horizontal pulse from the vertical interval. The signal V_{C3} output from the comparator **CP16** is directed to the multivibrator **402**, where V_{C3} triggers the B input of **402** to set a low level at its /Q output. The width of this low level is set by a capacitor **C19** (0.001 μf) and a resistor **R39** (11.3KΩ). In this case, the low level lasts 6–10 μs. The 6 μs lower time limit is chosen to be greater than the horizontal synchronizing pulse duration. The upper time limit is chosen so that the pulse will not get into active video signal.

The /Q output of **402** triggers the B input of the multivibrator **403** so as to set a high level output at its Q output. The duration of the high level at the Q output of **403** is determined by a capacitor **C20** (0.001 μf) and the combination of resistors **R40** (68KΩ) and **R41** (50KΩ). The position of switch SW_U is determined by the operation mode. For example, under the NTSC video signal, SW_U is open so that the duration of the high level at the Q output of **403** is set by **R40** and **C12**, for example 35 μs–50 μs. On the other hand, if the apparatus **100** of the present invention is for processing the HDTV video signal, the switch SW_U is closed so the **R41** is shunted across **R40**. Accordingly, the duration of the high level at the Q output of **403** is determined by **C20** and shunted resistors **R40** and **R41**, for example 17 μs–20 μs.

The Q output of **403**, along the /Q output of **402**, is coupled to inputs of an OR gate **03**. The output of OR gate **03** is the OR of the outputs of the multivibrators **402** and **403**. This output of O3 coincides with the synchronizing tip but lasts a little longer. The output of **03** is directed to an OR gate O4. Another input of the OR gate O4 receives the output from OR gate O2. The OR gate **04** serves to eliminate the half horizontal pulses during the vertical intervals, thereby producing a horizontal synchronizing output H_S.

A multivibrator **404** is used to generate a horizontal square waveform output H_Q. The output H_S of the OR gate O4 is coupled to the B input of **404** via the switch SW_T. When the apparatus **100** of the present invention operates under the HDTV video signal, the rising edges of output H_S triggers **404** at the B input to set a high level output at its Q output. Meanwhile, the switch SW_L is closed so that the positive 5V is applied to **404** via shunted resistors R42 and **R43** and a capacitor **C21**. Accordingly, the duration of the high level depends on a capacitor C21 and the resistance of shunted resistors R42 and R43. If the capacitance of C21 is set as 0.001 μf and R42 and R43 are respectively set as 51KΩ, the duration is then 15 μs.

If the apparatus **100** of the present invention operates with NTSC video signal, the output H_S is reversed by an inverter **I9** so that the B input of **404** is triggered by the falling edges of the synchronizing pulse, setting a high level at its Q output. At the same time, the switch SW_L is open so that the positive 5V voltage is applied to **404** via only a resistor R42. Assuming R42 has the resistance of 51KΩ and C21 has the capacitance of 0.001 μf, the duration of the high level of the Q output of **404** is 30 μs.

The output C_S of OR gate **02** is also directed to a vertical synchronizing filter circuitry including operational amplifiers **OP17** and **OP18**. A resistor **R44** of 37.4KΩ and a capacitor **C22** of 0.001 μf bridge across the output and negative input of OP17 to form a first stage integrator type low pass filter. The positive input of OP17 is tied to ground. The composite synchronizing output C_S is coupled to the negative input of OP17 via a resistor **R52** of 39KΩ. This configuration acts as a current source and leaky integrator such that the integrator is charged by the vertical broad pulses. The output from OP17 is coupled to the negative input of OP18 via a 10KΩ resistor **R50**. The positive input of OP18 is tied to ground. A resistor **R45** (10KΩ) and a capacitor **C15** (0.001 μf) are shunted across the negative input and the output of OP18, thereby providing a second stage integrator type low pass filter. Of course, a more traditional low pass filter circuit may be implemented by the addition of source resistors as shown in FIG. **11**.

This vertical filter circuitry employs a design which is an integrator and current source type, offsetting conventional optimal design. This design provides a frequency response characteristic without matching standard filter design curves which are commonly known. However, it is this design that provides a frequency response characteristic good for vertical synchronizing separation of the NTSC or HDTV video signal. This frequency response of the filter circuitry is shown in FIG. **6**.

Alternatively, other vertical separation circuits which utilize the duty cycle of the vertical sync pulse may be utilized as well.

The filter signal is applied to a positive input of a comparator **CP19** via a 38KΩ resistor **R51**. A resistor **R46** of 3.3KΩ is bridged between the positive input and output of CP19 to provide positive feedback hysteresis for CP19. A positive 5V voltage is tied to ground via resistors **R47** and **R48**. R47 has resistance of 20KΩ and **R48** has resistance of 10KΩ. A capacitor **C16** of 0.1 μf is shunted across resistor **R48**, thereby providing a stable reference voltage to the negative input of CP19. Furthermore, a positive 5V voltage is applied to the output of CP19 via a resistor **R49** (1KΩ). Filter circuitry provides a vertical synchronizing output V_S via CP19 and inverted by an inverter **I10**.

To obtain a field synchronizing output, the vertical synchronizing output from CP19 is directed to a flip-flop **405**. The clear input CLR and set input PR of **405** are coupled to a positive 5V. The CK input of **405** receives vertical sync and the D input of **405** is coupled to H sync square wave the /Q output of multivibrator **404**. The rising edges of the V_S pulses activate the trigger **405** to produce the field synchronizing output F_S. Upon arrival of the rising edges, the Q output of **405** is set to a level the same as that as its D input. In addition, an inverter **I11** is provided for outputting a reversed composite synchronizing output C_S.

A processing method **700** for synchronizing pulses of the video signals is shown in FIG. **7**. At step **701**, the video signal is sliced to produce synchronizing pulses. The video signal is then sampled in response to the sliced sync to precisely sense the sync tip peaks pulses, at step **702**, thereby providing two peak signal values representing the positive and negative peak values of each synchronizing pulse.

The peak signal values are further converted, at step **703**, into three reference signals which respectively represent the different levels relative to each synchronizing pulse. In particular, the three reference levels respectively represent the middle, upper and lower middle levels of the synchronizing pulse. Comparison of the three reference levels and the video signal is conducted at step **704**. As a result of this comparison, the logic pulse outputs are obtained. Step **705** is for restoring synchronizing pulses of the video signal by combining the logic outputs.

FIGS. **8–11** show a more detailed schematic circuit of a preferred embodiment in accordance with the present invention. All of the components in FIGS. **8–11** correspond directly to those presented in FIGS. **2–4**. The differences between FIGS. **2–4** and **8–11** include that all of components in FIGS. **8–11** are marked with commercial identification

US005754250A

United States Patent [19]

Cooper

[11] Patent Number: 5,754,250

[45] Date of Patent: *May 19, 1998

[54] **SYNCHRONIZING SIGNAL SEPARATING APPARATUS AND METHOD**

[76] Inventor: **J. Carl Cooper**, 15288 Via Pinto, Monte Sereno, Calif. 95030

[*] Notice: The term of this patent shall not extend beyond the expiration date of Pat. No. 5,486,869.

[21] Appl. No.: **566,484**

[22] Filed: **Dec. 4, 1995**

Related U.S. Application Data

[63] Continuation-in-part of Ser. No. 493,661, Jun. 22, 1995, abandoned, which is a continuation-in-part of Ser. No. 165,688, Dec. 13, 1993, Pat. No. 5,486,869.

[51] **Int. Cl.**[6] **H04N 5/08**

[52] **U.S. Cl.** **348/525**; 348/521

[58] **Field of Search** 348/525, 529, 348/530, 531, 521, 524; 375/113; 307/351; 358/153, 154, 155, 156, 157; H04N 5/08, 5/10

[56] **References Cited**

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58-178669	10/1983	Japan	H04N 5/08
58-186270	10/1983	Japan	H04N 5/08
1143241	2/1969	United Kingdom	H04N 5/08
2200011	12/1987	United Kingdom	H04N 5/08

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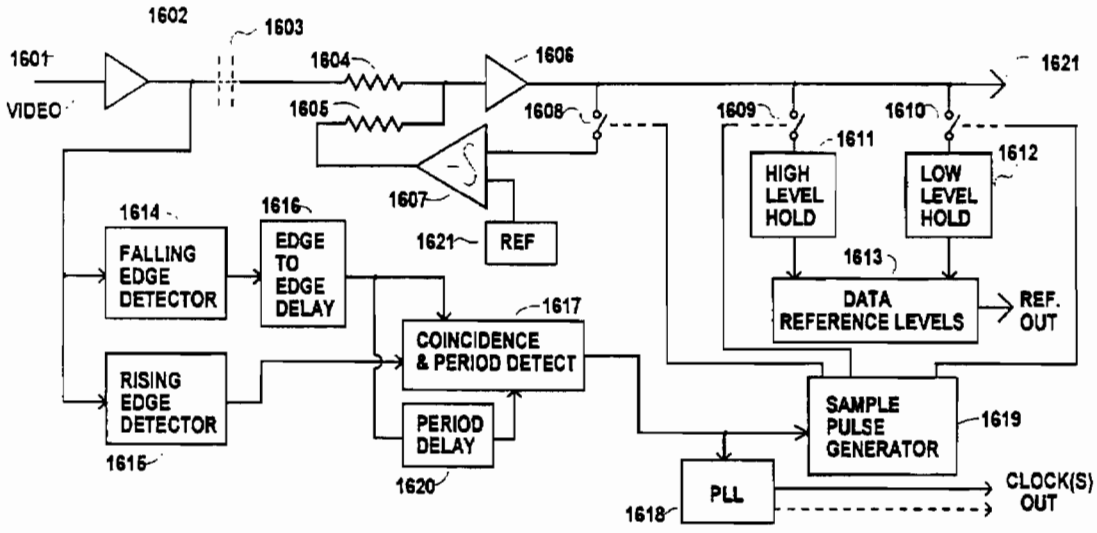
Primary Examiner—John K. Peng
Assistant Examiner—Chris Grant
Attorney, Agent, or Firm—J. Carl Cooper

[57] **ABSTRACT**

This invention is a method and apparatus for identifying and separating the synchronizing signal component of video like signals by identifying or detecting the arrangement or sequence of the known occurances of events or patterns of the sync. The invention also provides for establishing data slicing references in response to the levels of known portions of the sync component.

45 Claims, 15 Drawing Sheets



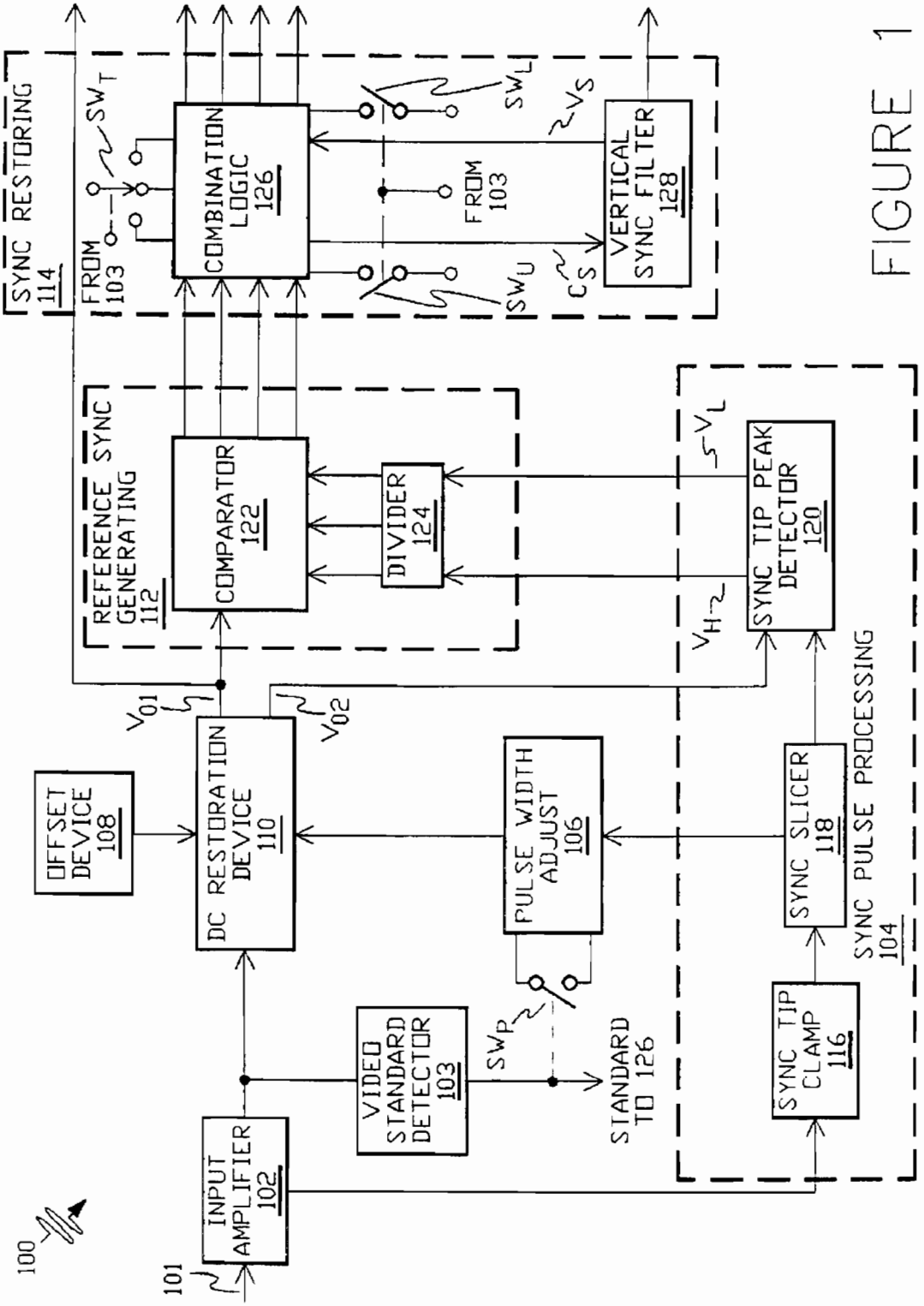
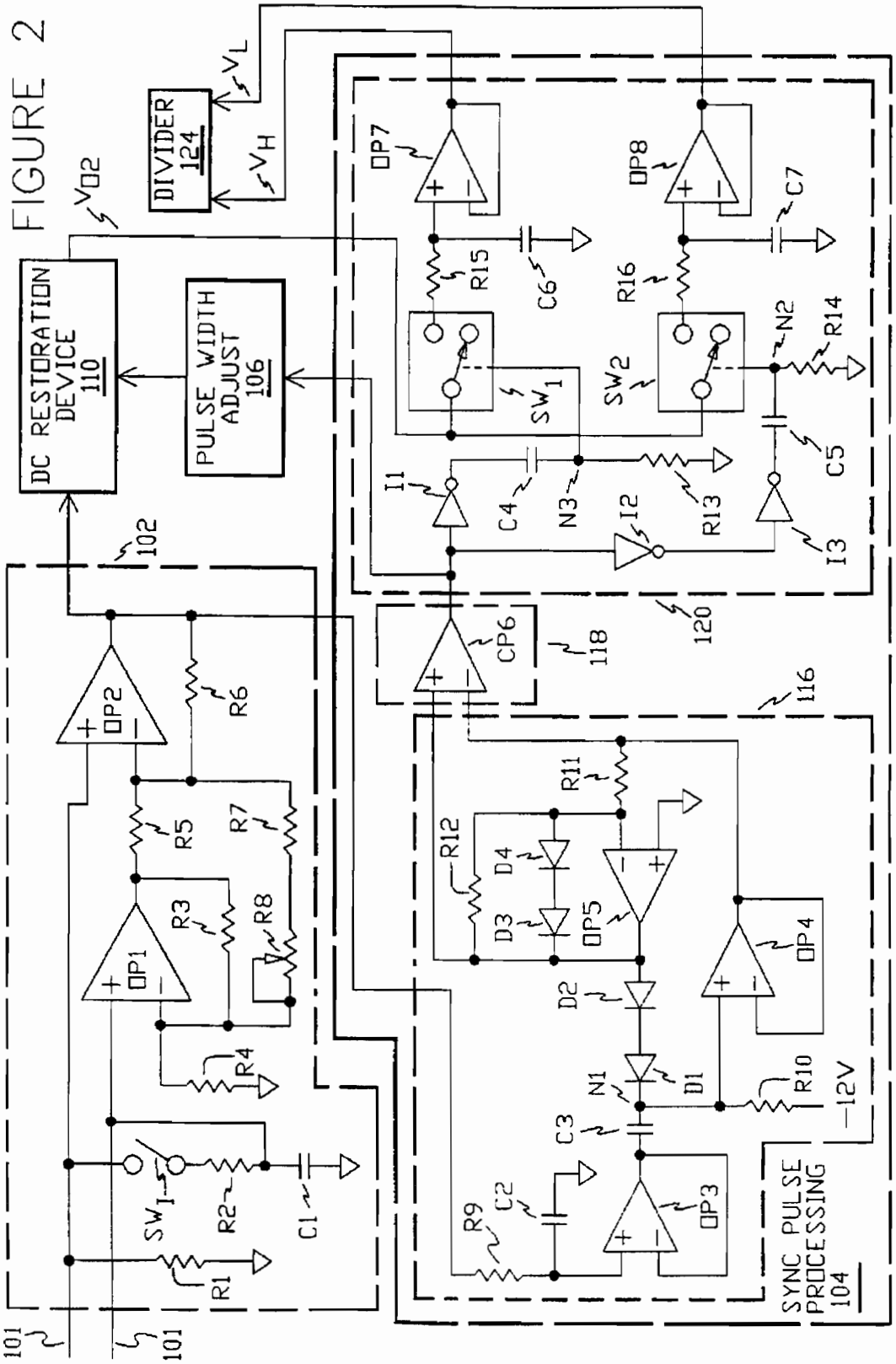

SYNC RESTORING 114
FROM 103
SW_T
COMBINATION LOGIC 126
FROM 103
SW_L
SW_U
V_S
C_S
VERTICAL SYNC FILTER 128
REFERENCE SYNC GENERATING 112
COMPARATOR 122
DIVIDER 124
V_L
V_H
SYNC TIP PEAK DETECTOR 120
V_01
V_02
OFFSET DEVICE 108
DC RESTORATION DEVICE 110
PULSE WIDTH ADJUST 106
SYNC SLICER 118
SYNC PULSE PROCESSING 104
SW_P
VIDEO STANDARD DETECTOR 103
STANDARD TO 126
SYNC TIP CLAMP 116
INPUT AMPLIFIER 102
100
101

FIGURE 1

FIGURE 2


DIVIDER 124
V_L
V_H
V_{02}
DC RESTORATION DEVICE 110
PULSE WIDTH ADJUST 106
102
OP7
OP8
C7
R15
C6
R16
N2
R14
SW1
SW2
C5
I1
C4
N3
I2
R13
I3
120
CP6
118
116
OP2
R6
R11
R5
R7
R12
D4
D3
OP5
R3
R8
OP1
OP4
D2
R4
N1
D1
R10
-12V
C3
SW1
R2
C1
R9
C2
OP3
SYNC PULSE PROCESSING 104
101
101

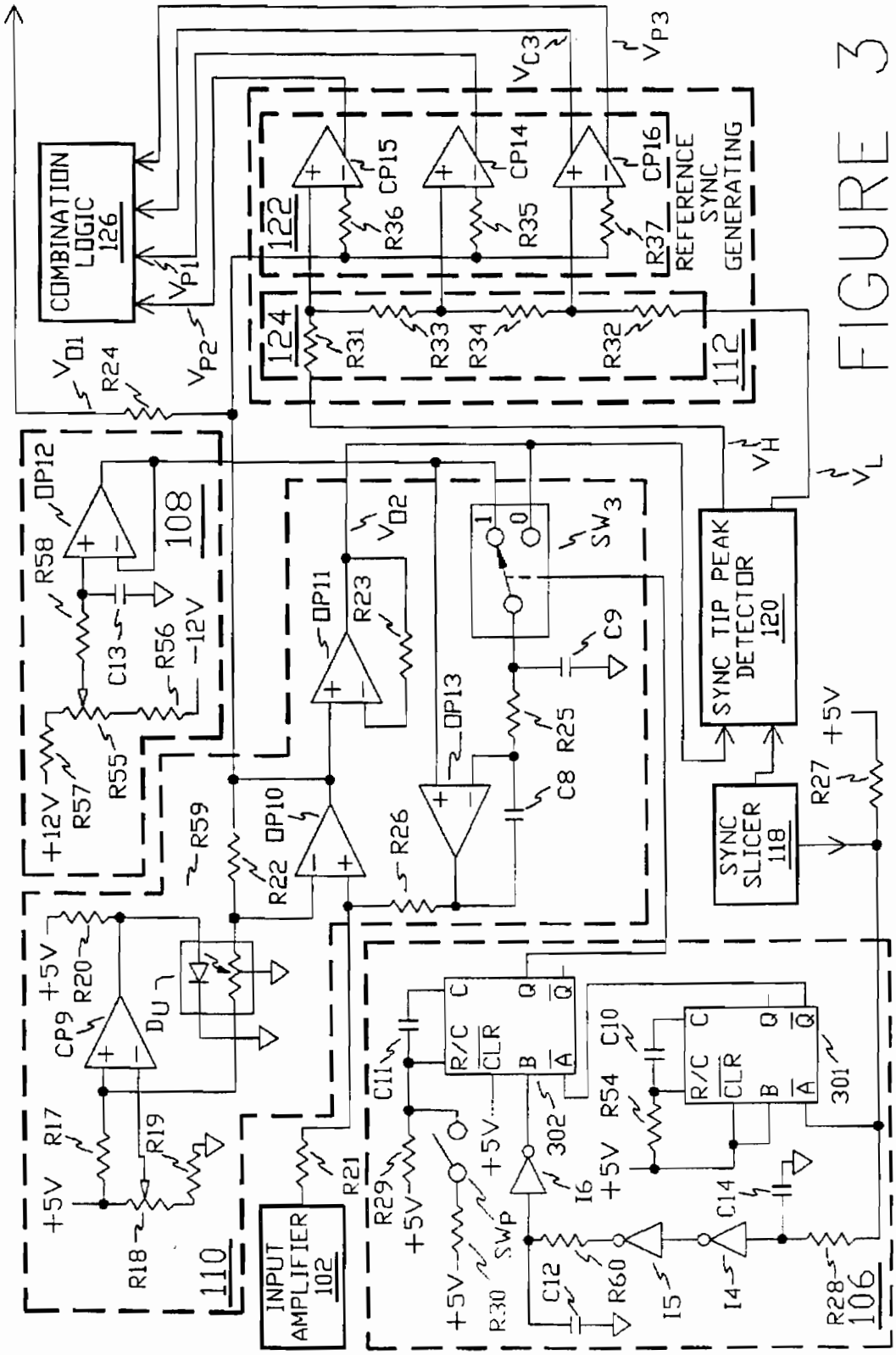
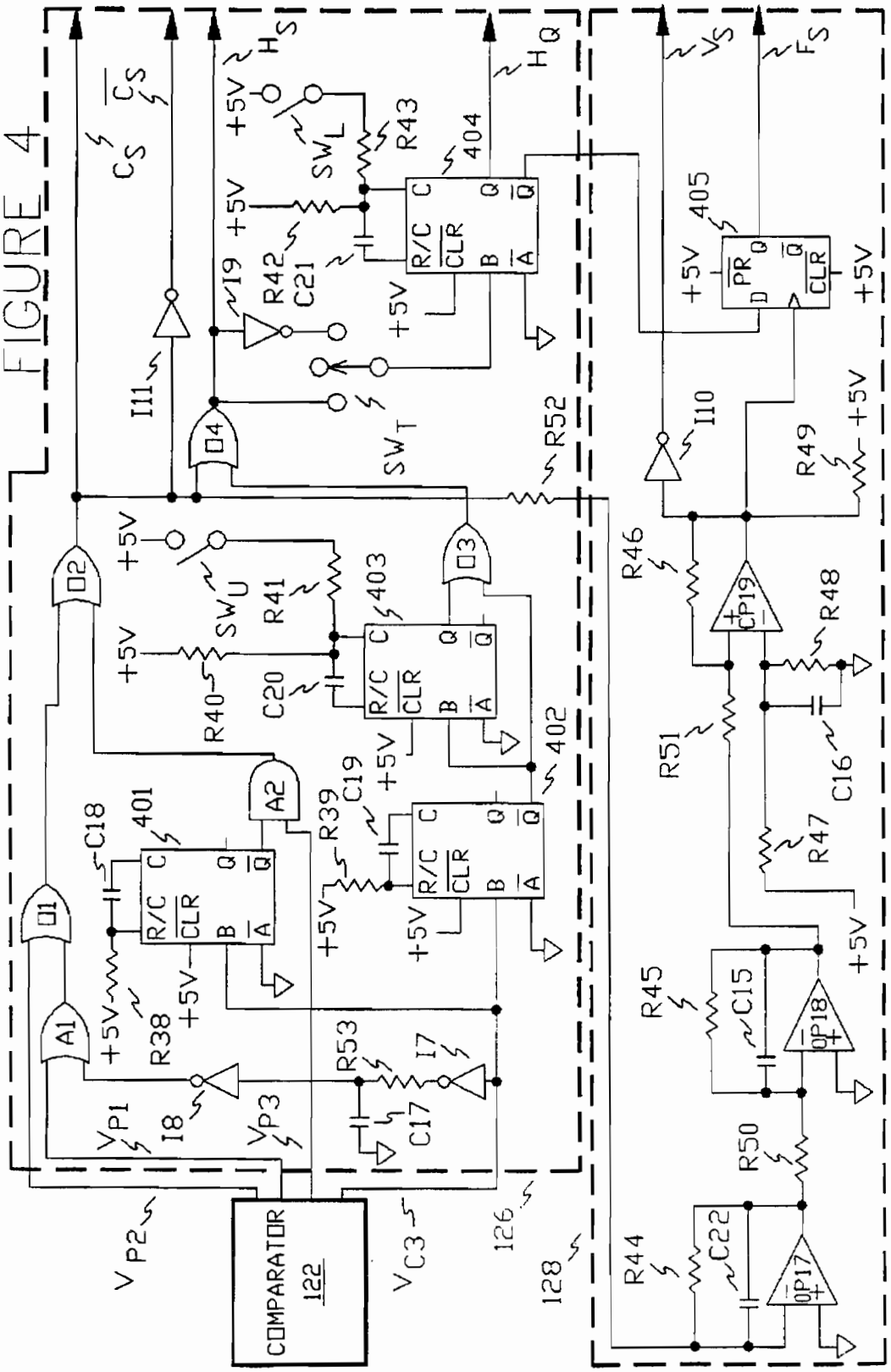

COMBINATION LOGIC 126
122
CP15
CP14
CP16
R36
R35
R37
REFERENCE SYNC GENERATING
124
R31
R33
R34
R32
112
R24
108
OP12
R58
C13
R56
-12V
+12V
R57
R55
OP11
R23
OP10
R22
R59
OP13
R26
C8
R25
C9
SW3
SYNC TIP PEAK DETECTOR 120
SYNC SLICER 118
R27
+5V
110
INPUT AMPLIFIER 102
CP9
R20
DU
R17
R19
R18
R21
C11
R29
SWP
R30
302
I6
C10
R54
301
C12
R60
I5
C14
I4
R28
106

FIGURE 3

FIGURE 4


$\overline{CS}$
CS
HS
HQ
VS
FS
+5V
SWL
R43
404
R/C
CLR
C
Q
B
A
R42
C21
I19
405
PR
D
CLR
I11
SWT
R52
I10
R49
D4
D3
D2
D1
SWU
R41
403
R40
C20
402
R46
CP19
R48
R51
C16
R47
C19
R39
401
C18
A2
A1
R38
R53
I7
I8
VP1
VP3
R45
C15
OP18
R50
R44
C22
OP17
VP2
COMPARATOR
122
VC3
126
128

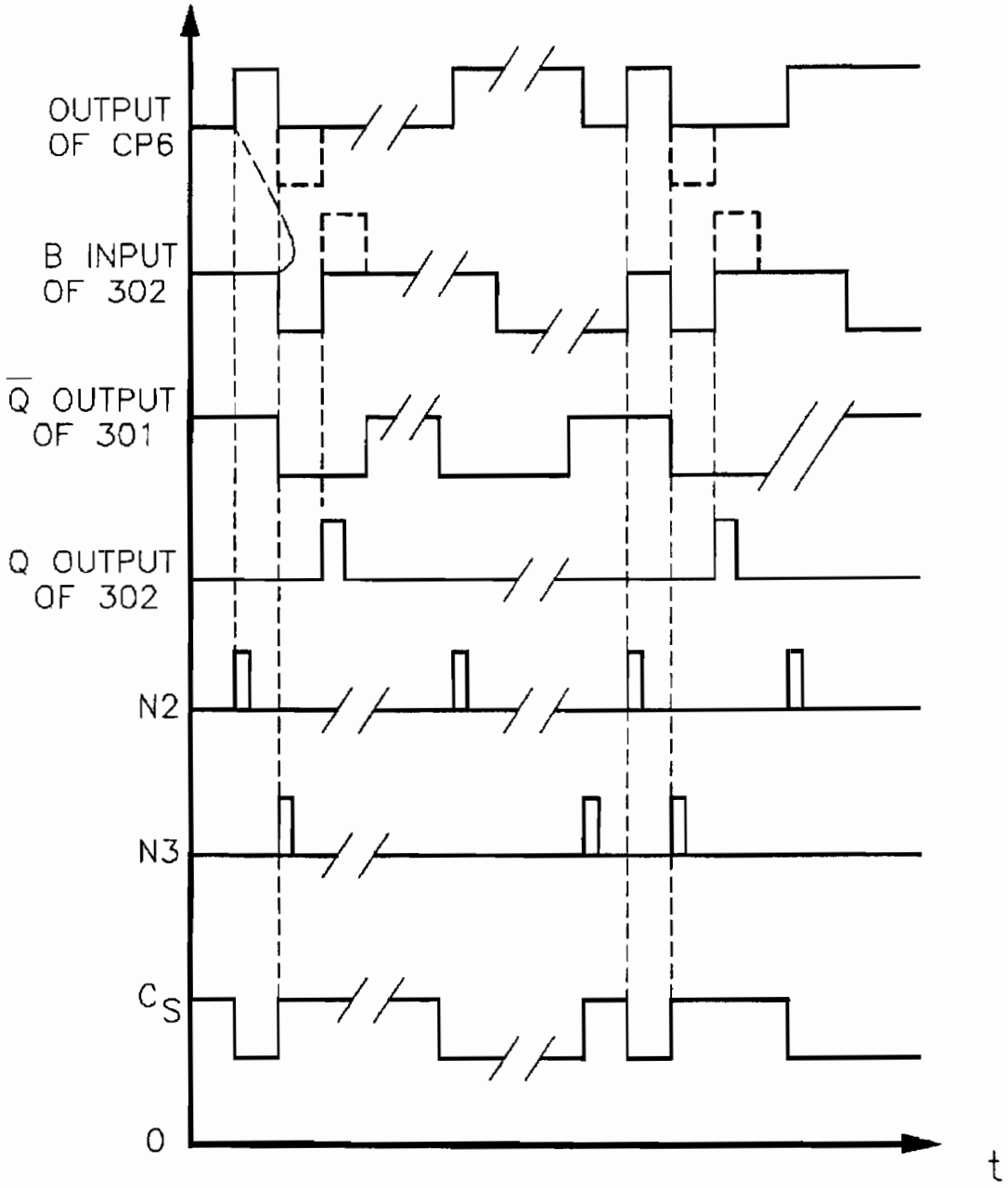

OUTPUT OF CP6
B INPUT OF 302
$\overline{Q}$ OUTPUT OF 301
Q OUTPUT OF 302
N2
N3
C_S
0
t

FIGURE 5

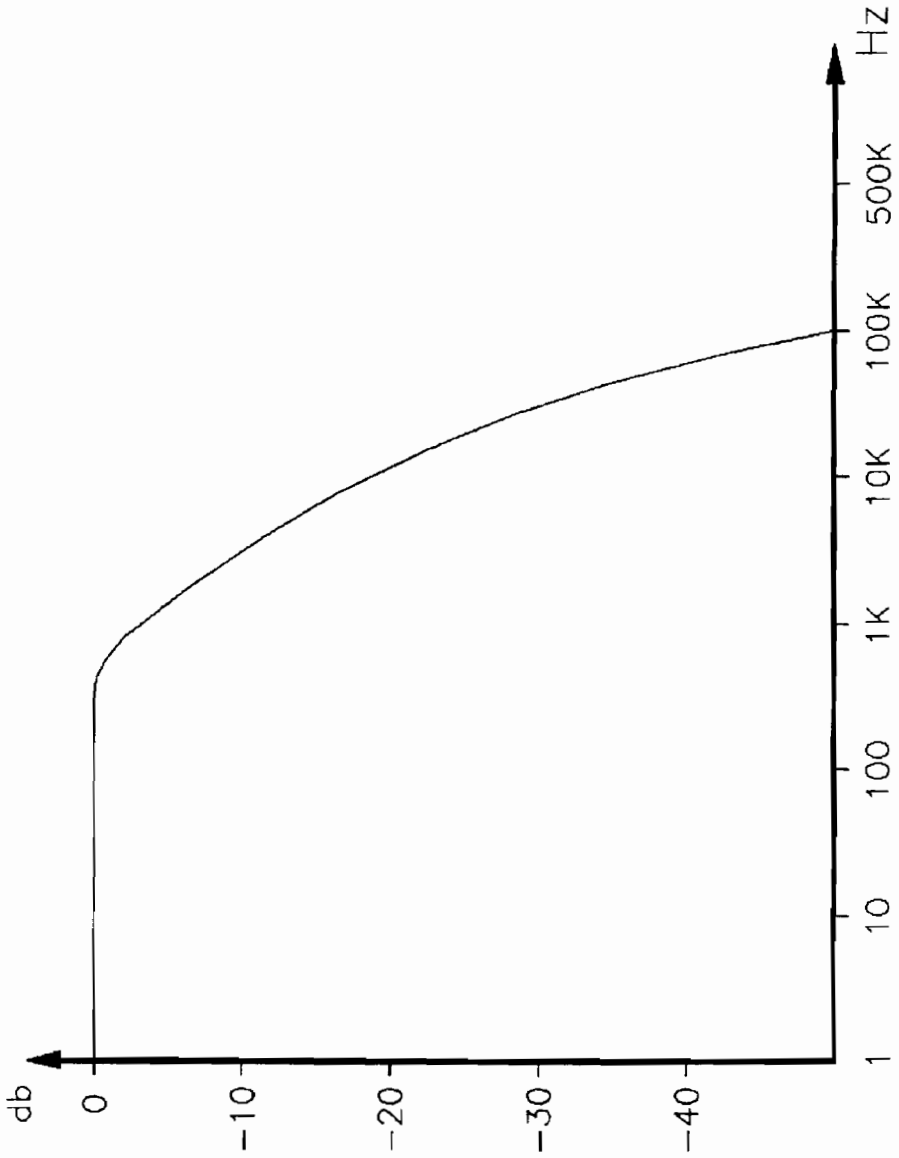


FIGURE 6

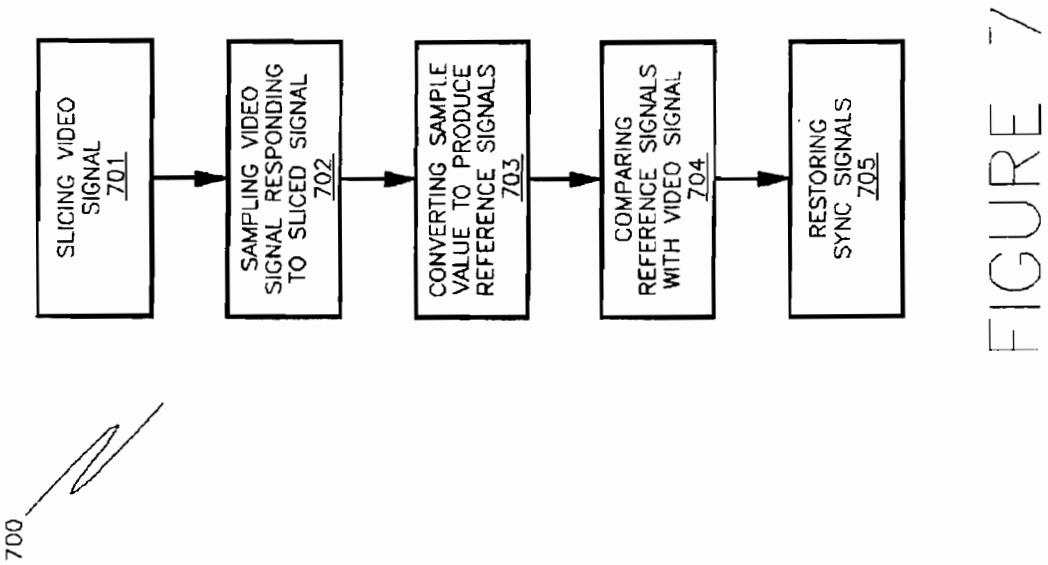

SLICING VIDEO SIGNAL 701
SAMPLING VIDEO SIGNAL RESPONDING TO SLICED SIGNAL 702
CONVERTING SAMPLE VALUE TO PRODUCE REFERENCE SIGNALS 703
COMPARING REFERENCE SIGNALS WITH VIDEO SIGNAL 704
RESTORING SYNC SIGNALS 705
700

FIGURE 7

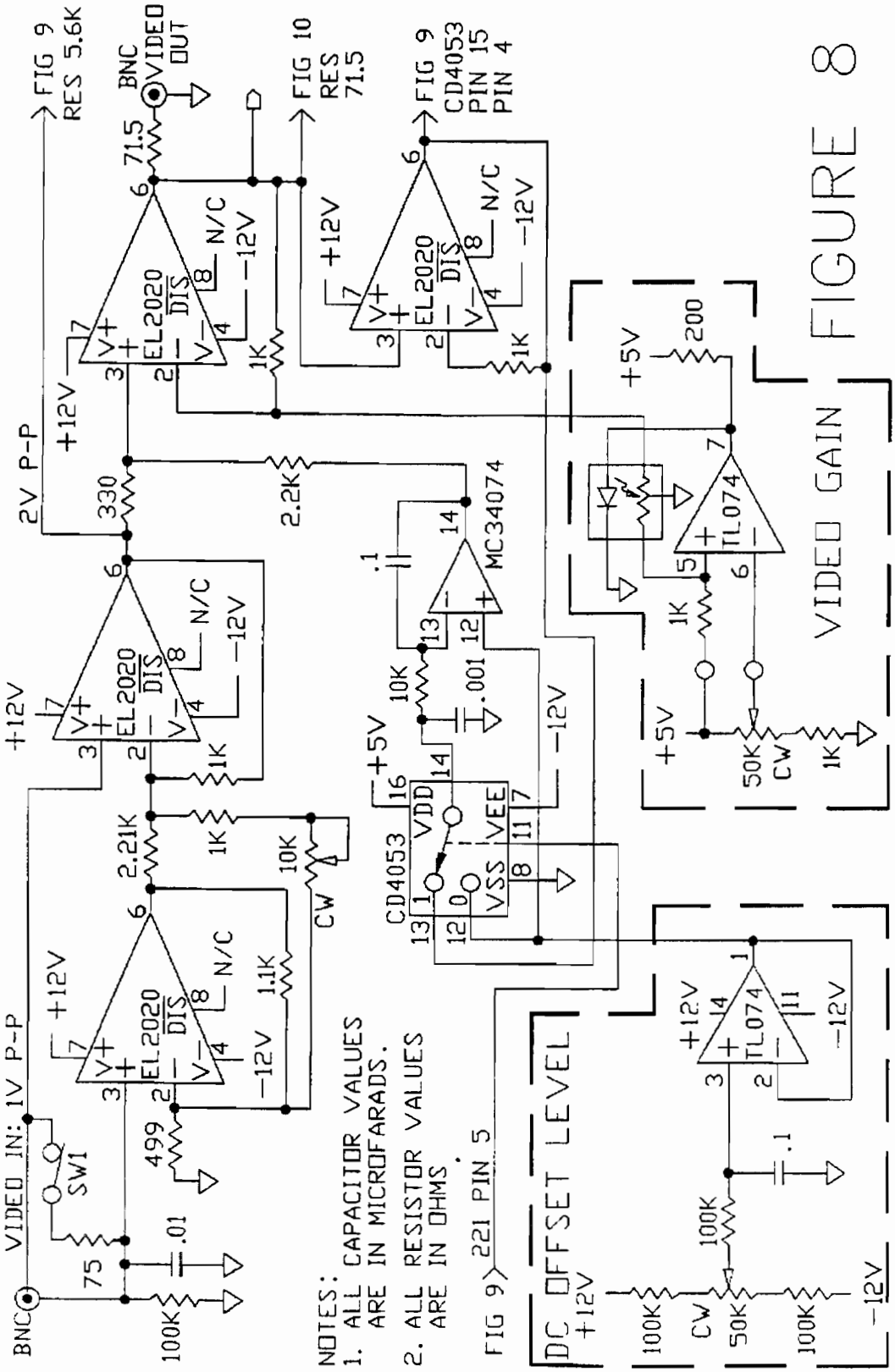


FIG 9 RES 5.6K
BNC VIDEO OUT
71.5
FIG 10 RES 71.5
FIG 9 CD4053 PIN 15 PIN 4
EL2020
DIS
N/C
+12V
-12V
1K
2V P-P
330
2.2K
MC34074
.1
10K
.001
+5V
200
TL074
50K CW
VIDEO GAIN
2.21K
10K CW
1.1K
CD4053
VDD
VSS
VEE
VIDEO IN: 1V P-P
SW1
75
499
.01
100K
BNC
NOTES:
1. ALL CAPACITOR VALUES ARE IN MICROFARADS.
2. ALL RESISTOR VALUES ARE IN OHMS.
FIG 9 221 PIN 5
DC OFFSET LEVEL
100K
CW
50K
FIGURE 8

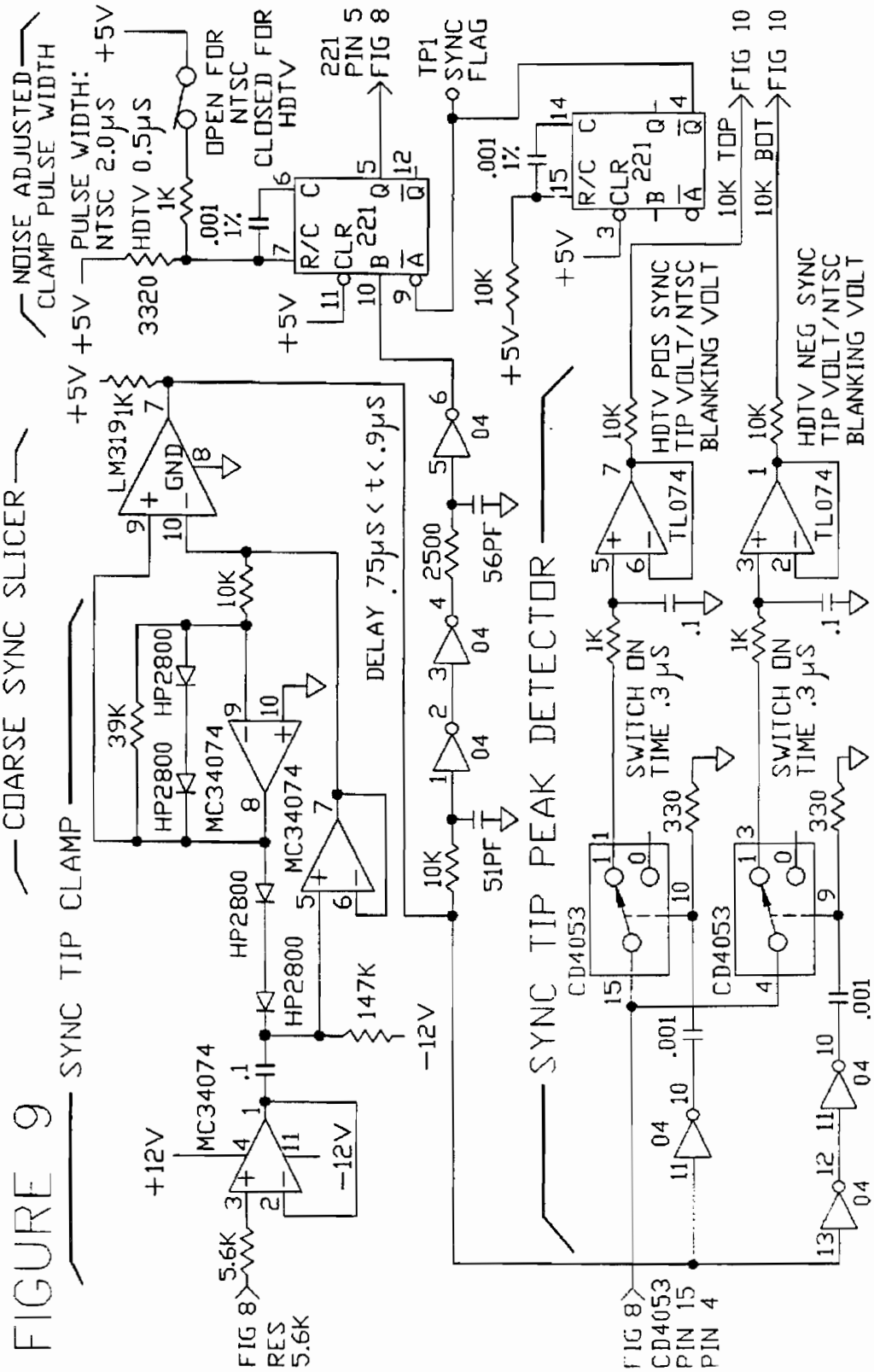

NOISE ADJUSTED CLAMP PULSE WIDTH
PULSE WIDTH: NTSC 2.0µS HDTV 0.5µS
+5V
3320
1K
.001 1%
OPEN FOR NTSC
CLOSED FOR HDTV
221
PIN 5 FIG 8
TP1 SYNC FLAG
R/C C
CLR
221
Q
A
B
COARSE SYNC SLICER
SYNC TIP CLAMP
LM319
GND
39K
HP2800
MC34074
10K
DELAY .75µS < t < .9µS
04
2500
56PF
51PF
147K
-12V
+12V
5.6K
FIG 8 RES 5.6K
SYNC TIP PEAK DETECTOR
CD4053
SWITCH ON TIME .3 µS
330
.1
.001
HDTV POS SYNC TIP VOLT/NTSC BLANKING VOLT
HDTV NEG SYNC TIP VOLT/NTSC BLANKING VOLT
TL074
10K TOP
10K BOT
FIG 10
FIG 8 CD4053 PIN 15 PIN 4
FIGURE 9

FIGURE 10

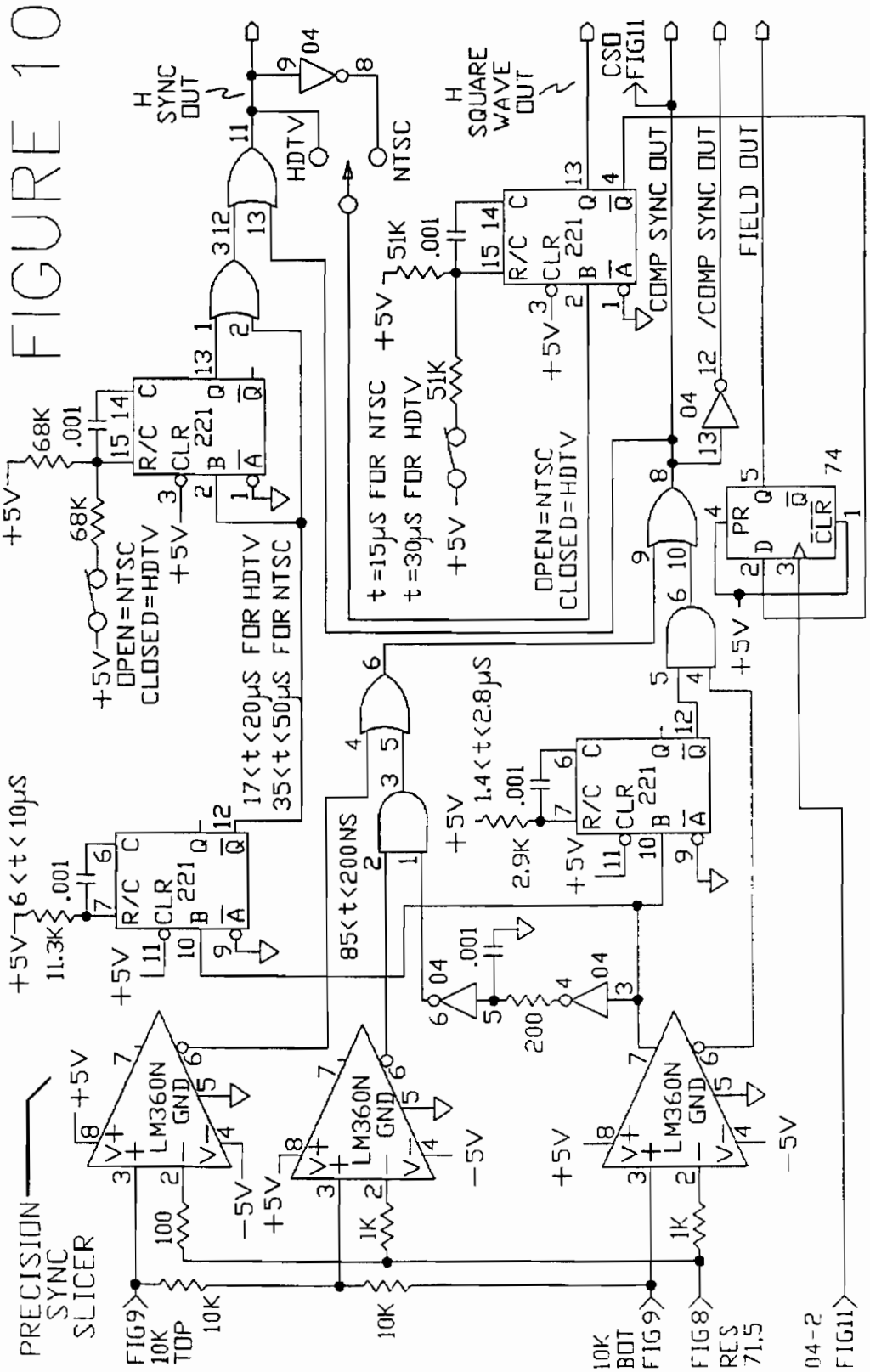
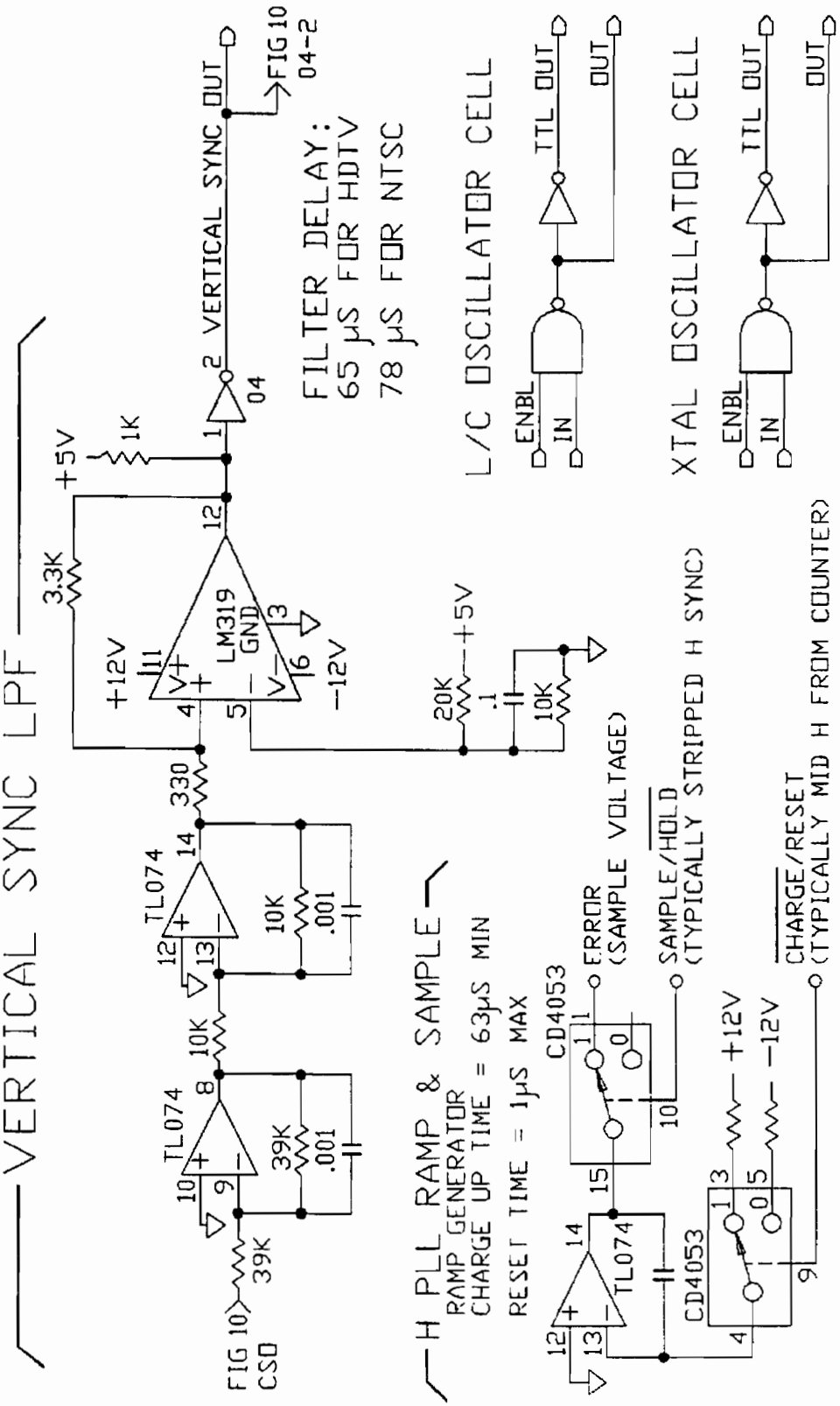

H SYNC OUT
HDTV
NTSC
H SQUARE WAVE OUT
CSD FIG11
COMP SYNC OUT
/COMP SYNC OUT
FIELD OUT
+5V
68K
.001
OPEN=NTSC CLOSED=HDTV
17<t<20µS FOR HDTV
35<t<50µS FOR NTSC
t=15µS FOR NTSC
t=30µS FOR HDTV
51K
OPEN=NTSC CLOSED=HDTV
6<t<10µS
11.3K
85<t<200NS
1.4<t<2.8µS
2.9K
200
LM360N
GND
100
1K
10K
PRECISION SYNC SLICER
FIG9 10K TOP
10K BOT FIG9
FIG8 RES 71.5
04-2 FIG11

FIGURE 11


VERTICAL SYNC LPF
+5V
1K
3.3K
+12V
LM319
GND
−12V
330
TL074
10K
.001
39K
FIG 10
CSD
2 VERTICAL SYNC OUT
FIG 10
04-2
FILTER DELAY:
65 µS FOR HDTV
78 µS FOR NTSC
L/C OSCILLATOR CELL
TTL OUT
OUT
ENBL
IN
XTAL OSCILLATOR CELL
20K
.1
10K
H PLL RAMP & SAMPLE
RAMP GENERATOR
CHARGE UP TIME = 63µS MIN
RESET TIME = 1µS MAX
CD4053
ERROR
(SAMPLE VOLTAGE)
SAMPLE/HOLD
(TYPICALLY STRIPPED H SYNC)
CHARGE/RESET
(TYPICALLY MID H FROM COUNTER)

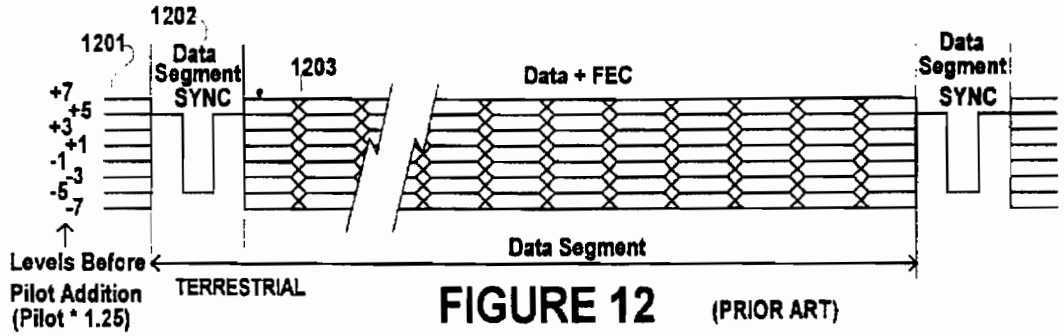


FIGURE 12 (PRIOR ART)

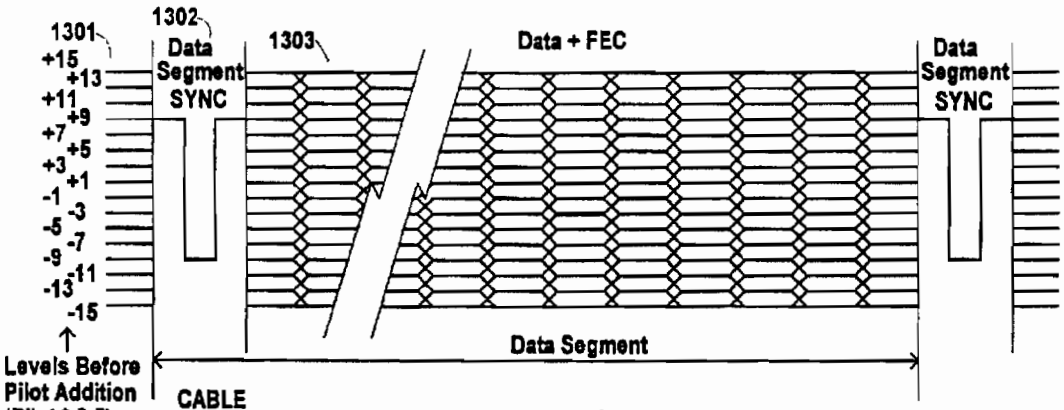


FIGURE 13 (PRIOR ART)

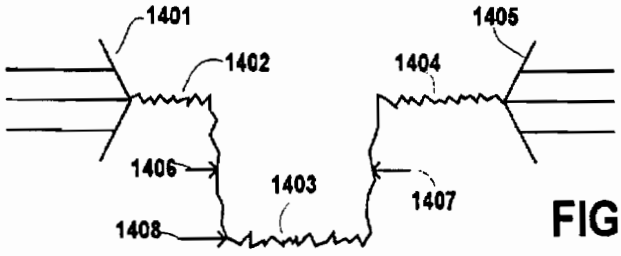


FIGURE 14

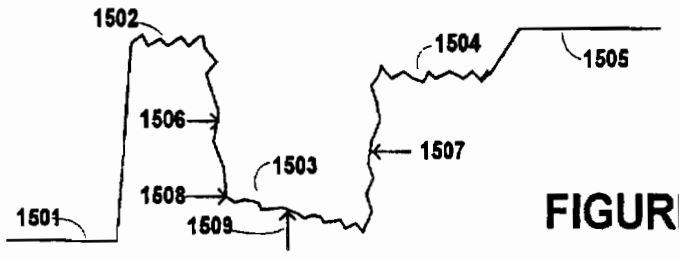


FIGURE 15

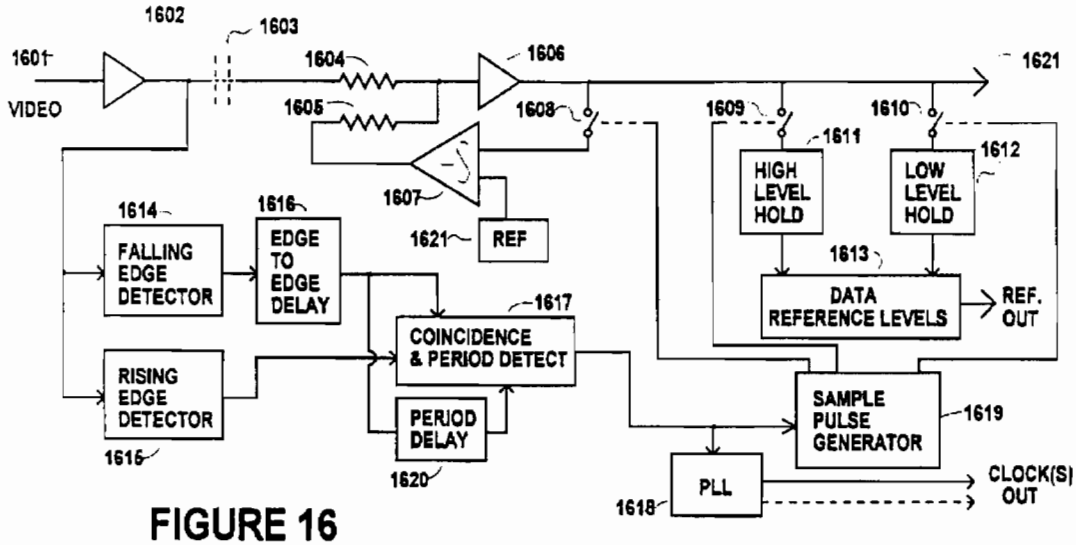


FIGURE 16

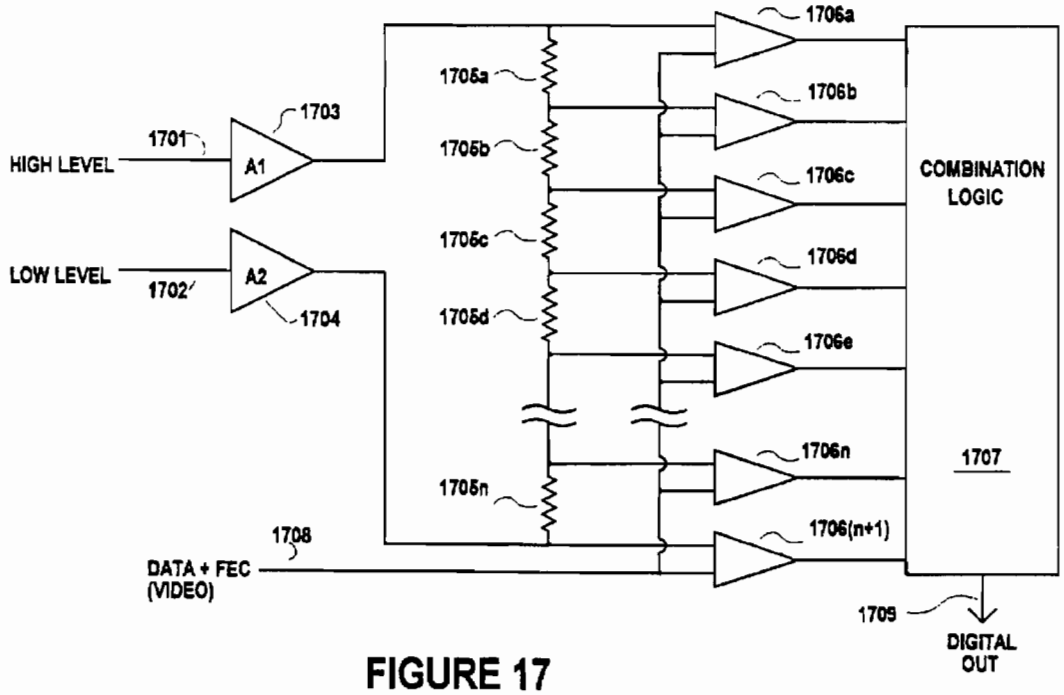


FIGURE 17

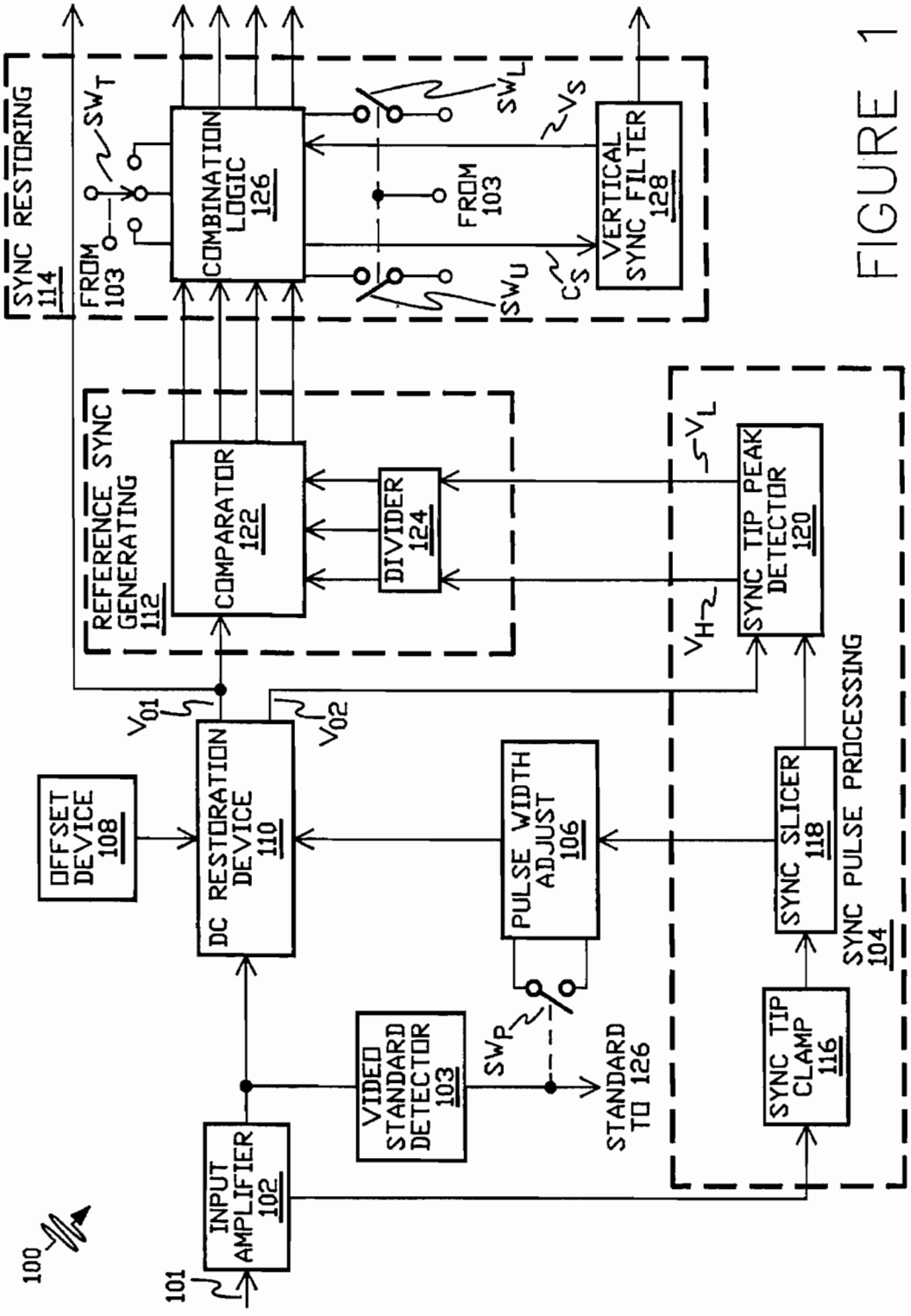
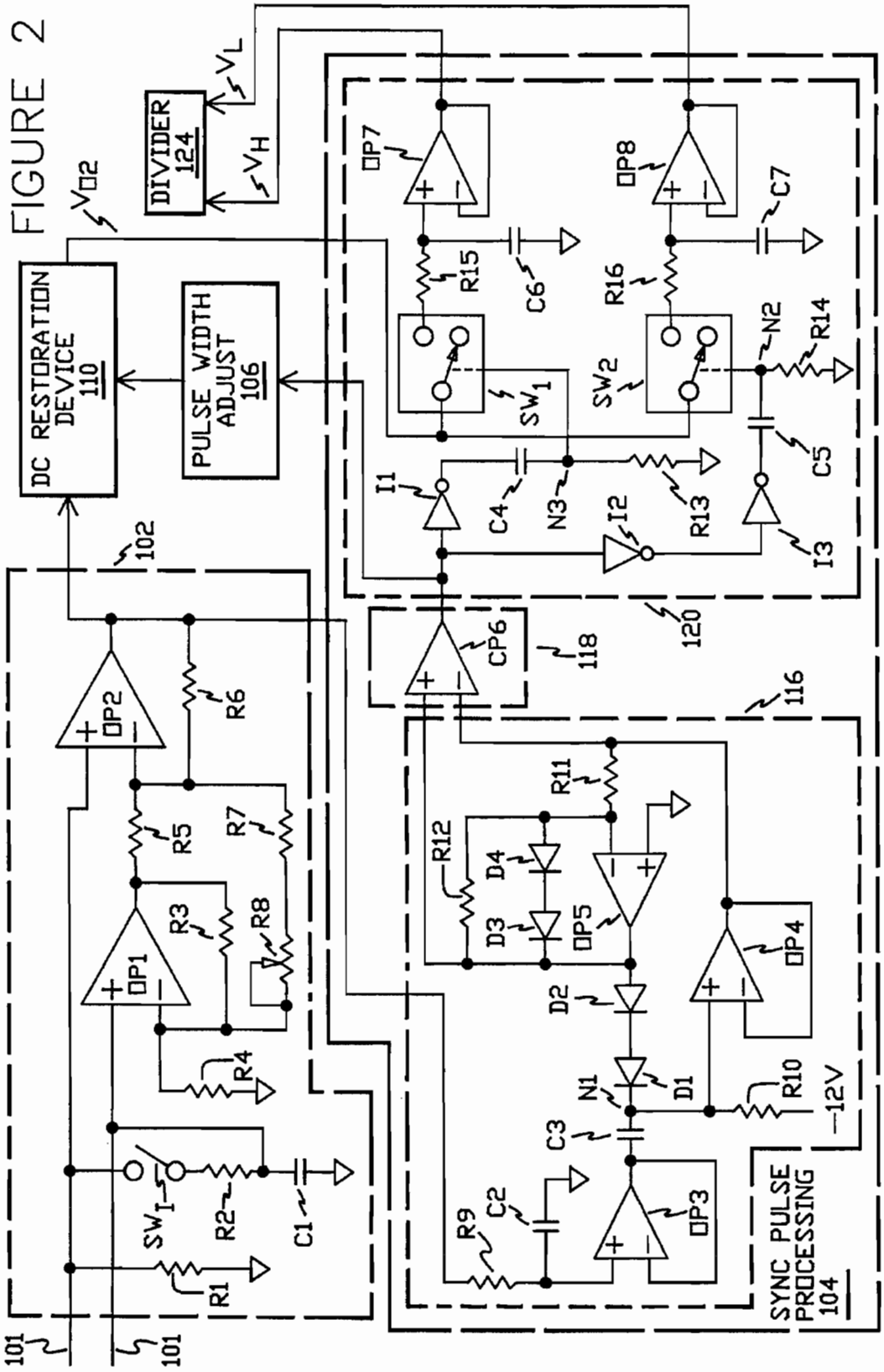

SYNC RESTORING 114
FROM 103
SW_T
COMBINATION LOGIC 126
SW_L
SW_U
FROM 103
V_S
C_S
VERTICAL SYNC FILTER 128
REFERENCE SYNC GENERATING 112
COMPARATOR 122
DIVIDER 124
V_L
V_H
SYNC TIP PEAK DETECTOR 120
V_01
V_02
OFFSET DEVICE 108
DC RESTORATION DEVICE 110
PULSE WIDTH ADJUST 106
SYNC SLICER 118
SYNC PULSE PROCESSING 104
VIDEO STANDARD DETECTOR 103
SW_P
STANDARD TO 126
SYNC TIP CLAMP 116
INPUT AMPLIFIER 102
100
101

FIGURE 1

FIGURE 2


DIVIDER 124
V_L
V_H
V_{D2}
DC RESTORATION DEVICE 110
PULSE WIDTH ADJUST 106
102
OP7
OP8
C7
R15
C6
R16
N2
R14
SW_1
SW_2
C5
I1
C4
N3
I2
R13
I3
120
CP6
118
116
OP2
R6
R11
R12
D4
D3
OP5
OP4
R5
R7
R3
R8
OP1
D2
R4
N1
D1
R10
-12V
C3
C2
R9
OP3
SW_1
R2
C1
R1
SYNC PULSE PROCESSING 104
101
101

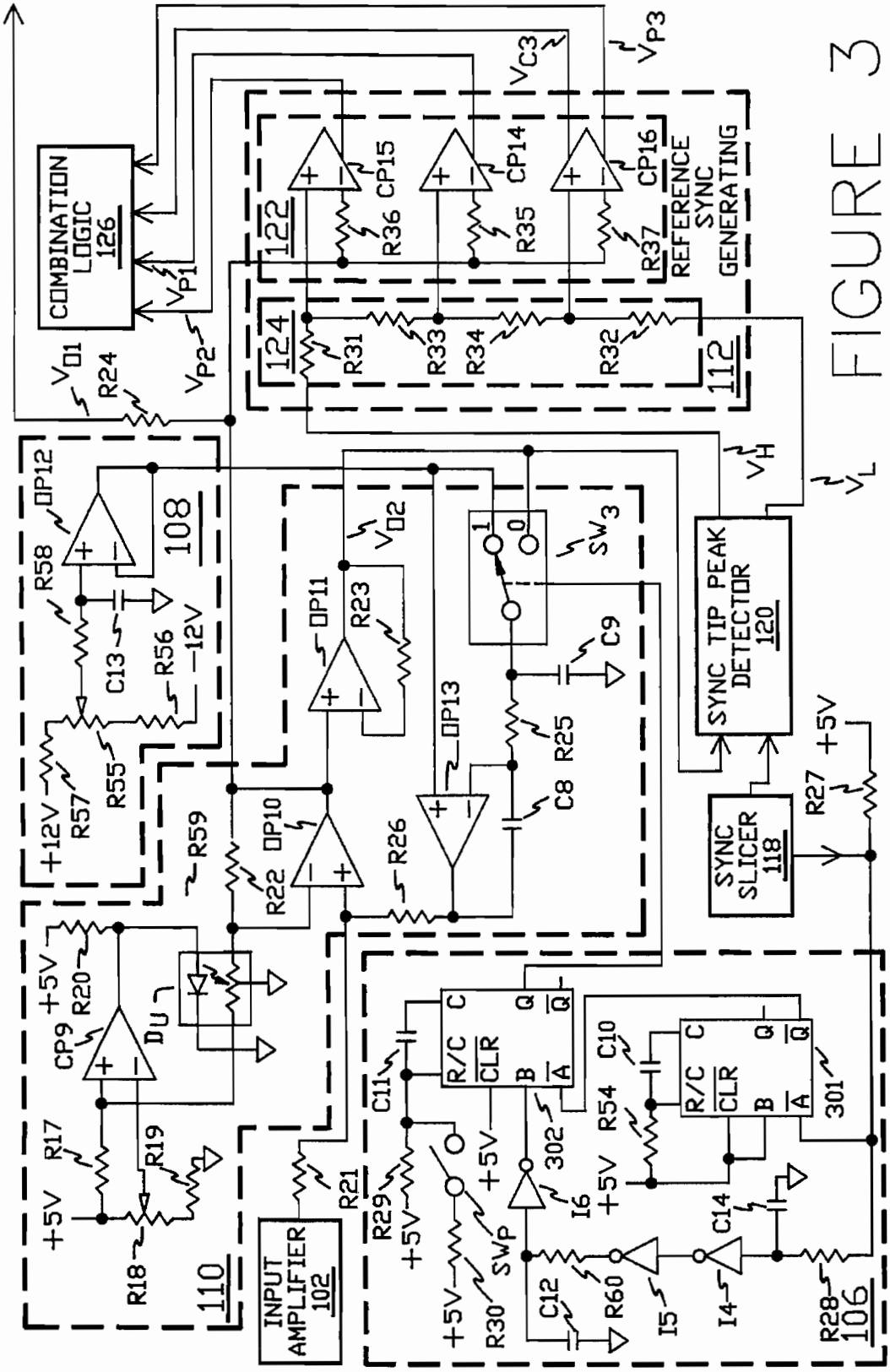
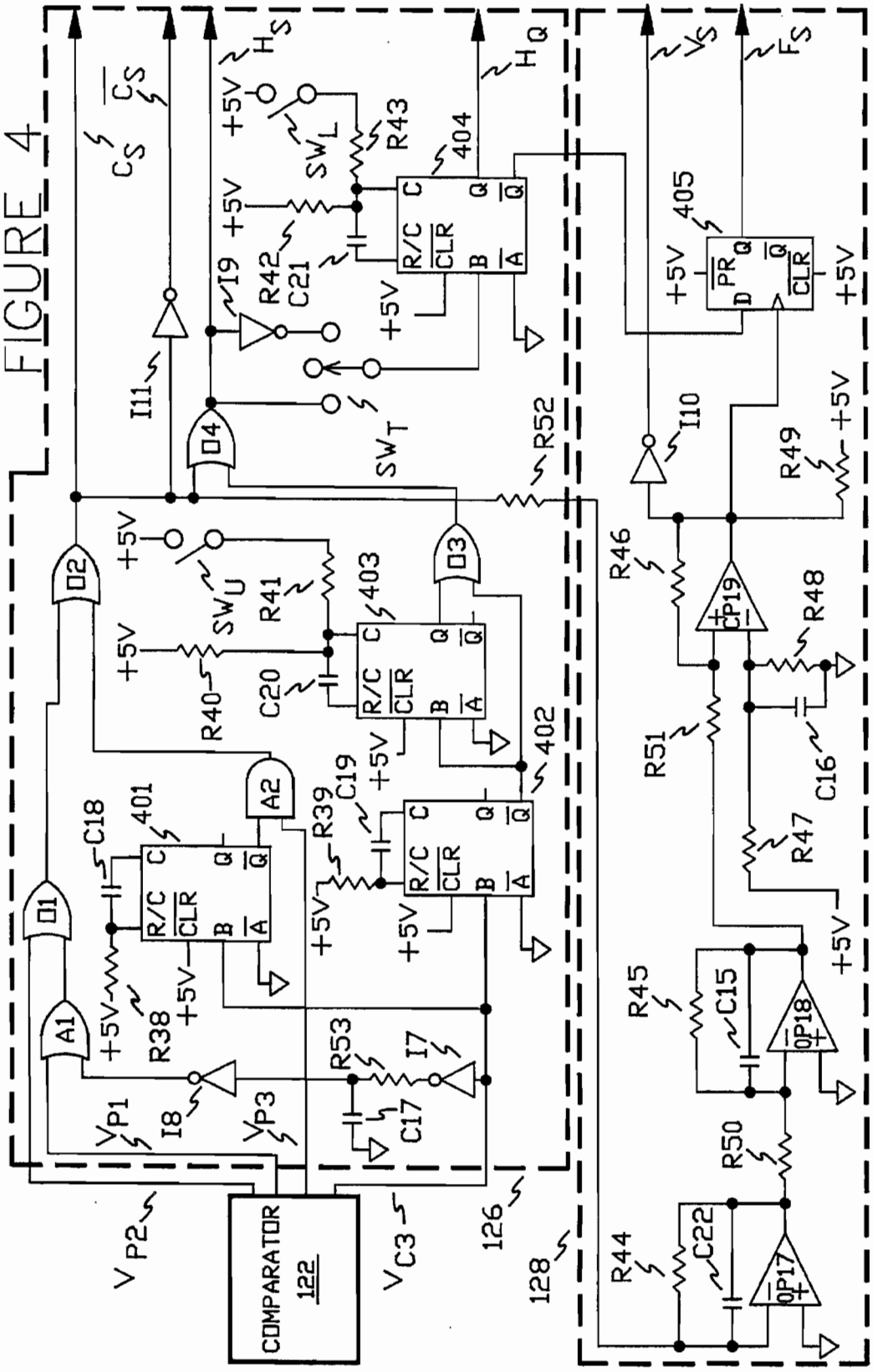

COMBINATION LOGIC 126
REFERENCE SYNC GENERATING
122
124
112
108
110
SYNC TIP PEAK DETECTOR 120
SYNC SLICER 118
INPUT AMPLIFIER 102
106
301
302
SW3
SWP
+5V
+12V
-12V

FIGURE 3

FIGURE 4


$\overline{CS}$
CS
HS
HQ
VS
FS
+5V
SWL
SWU
SWT
R43
R42
C21
I19
404
405
I11
D4
R52
I10
R49
D2
D3
R41
R40
C20
403
402
R46
CP19
R48
R51
C16
R47
C19
R39
401
C18
A2
D1
A1
R38
R53
I7
I8
C17
VP1
VP3
R45
C15
OP18
R50
R44
C22
OP17
VP2
VC3
126
128
COMPARATOR
122
R/C
CLR
PR
D
Q
A
B
C

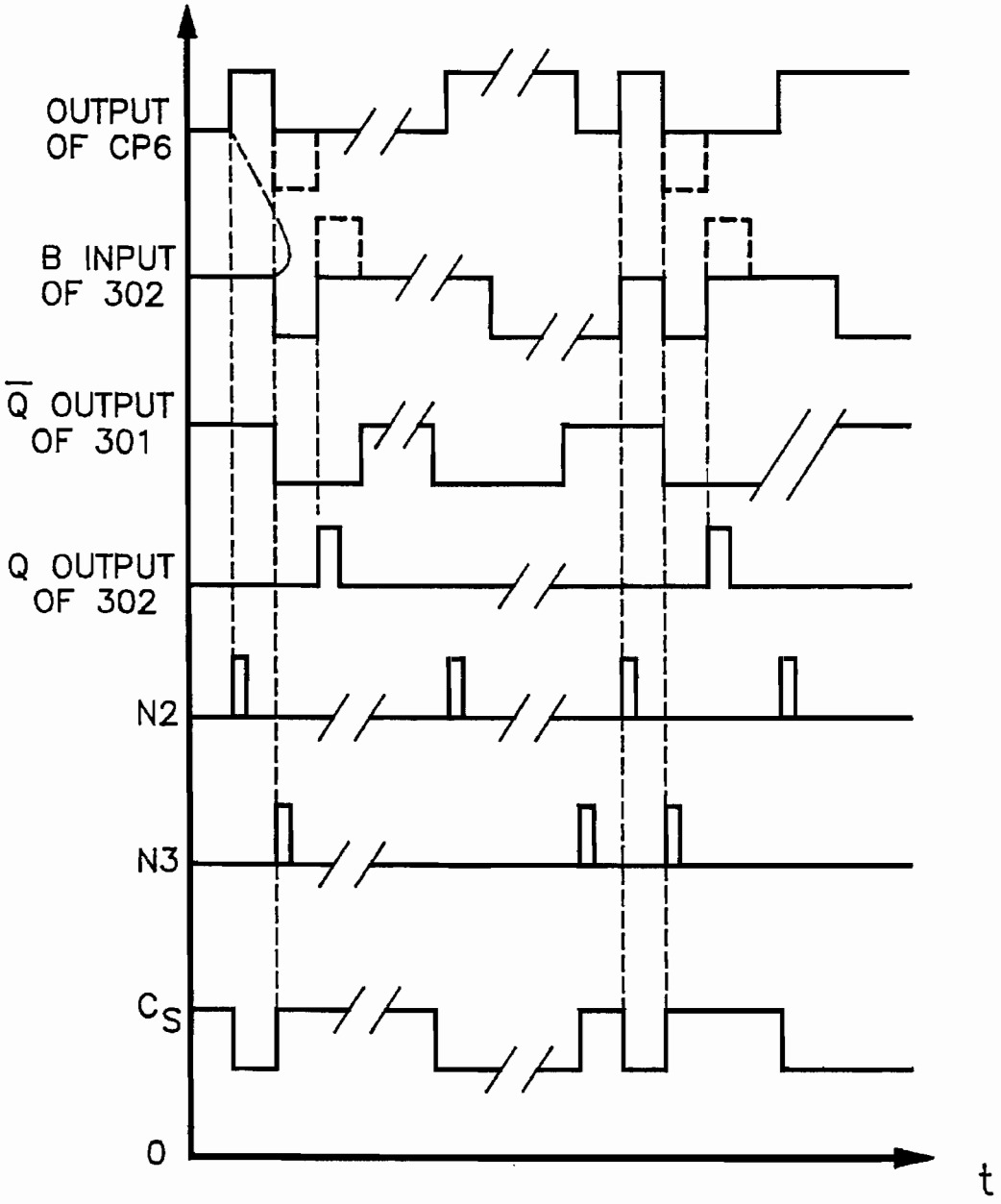

OUTPUT OF CP6
B INPUT OF 302
$\overline{Q}$ OUTPUT OF 301
Q OUTPUT OF 302
N2
N3
C_S
0
t

FIGURE 5

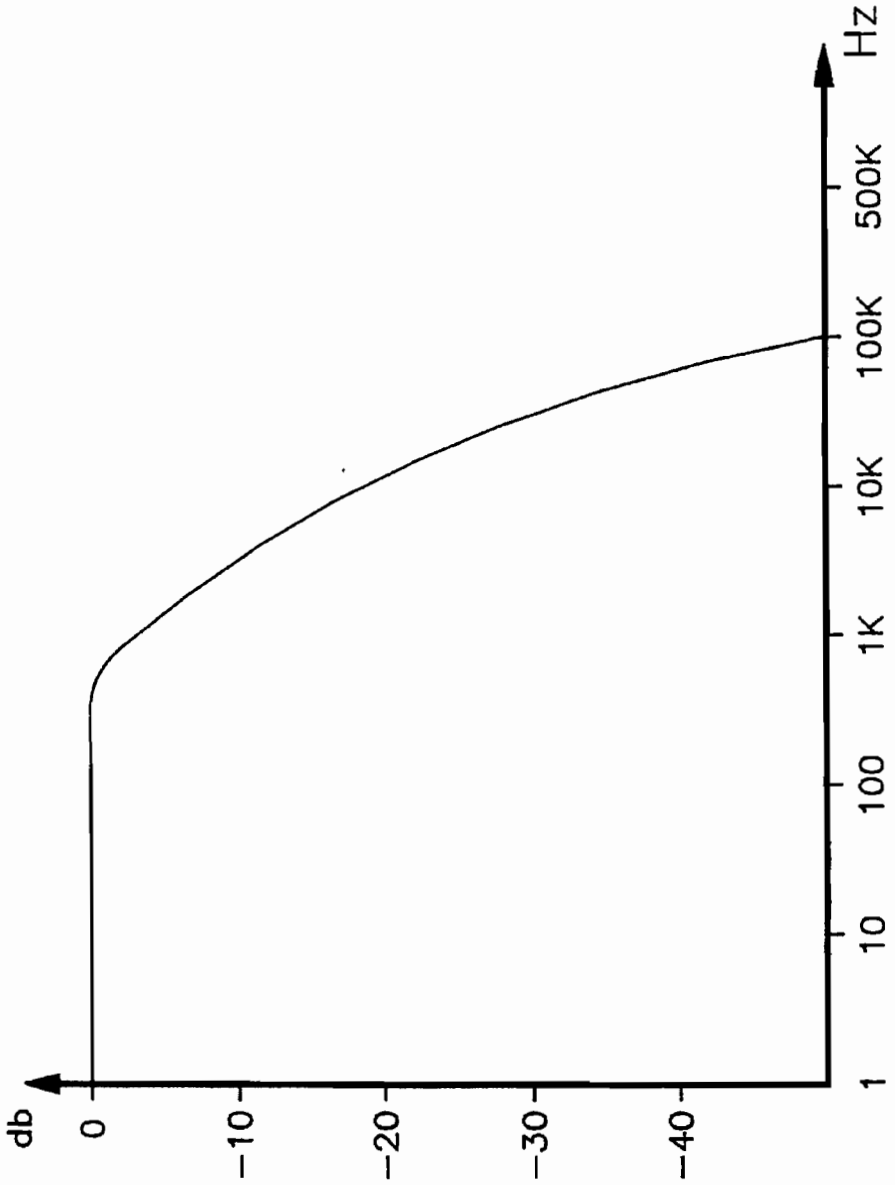


FIGURE 6

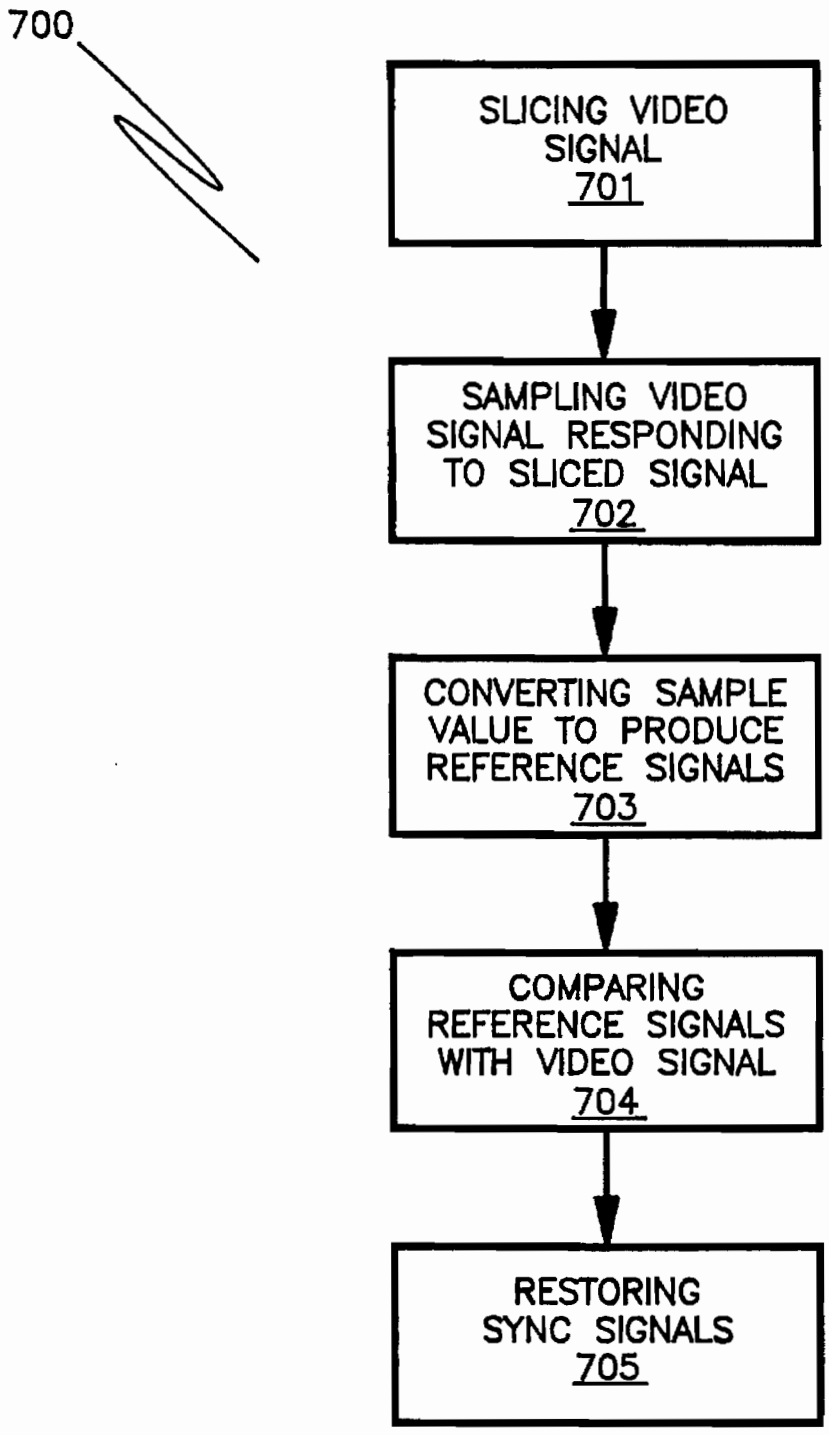

700
SLICING VIDEO SIGNAL 701
SAMPLING VIDEO SIGNAL RESPONDING TO SLICED SIGNAL 702
CONVERTING SAMPLE VALUE TO PRODUCE REFERENCE SIGNALS 703
COMPARING REFERENCE SIGNALS WITH VIDEO SIGNAL 704
RESTORING SYNC SIGNALS 705

FIGURE 7

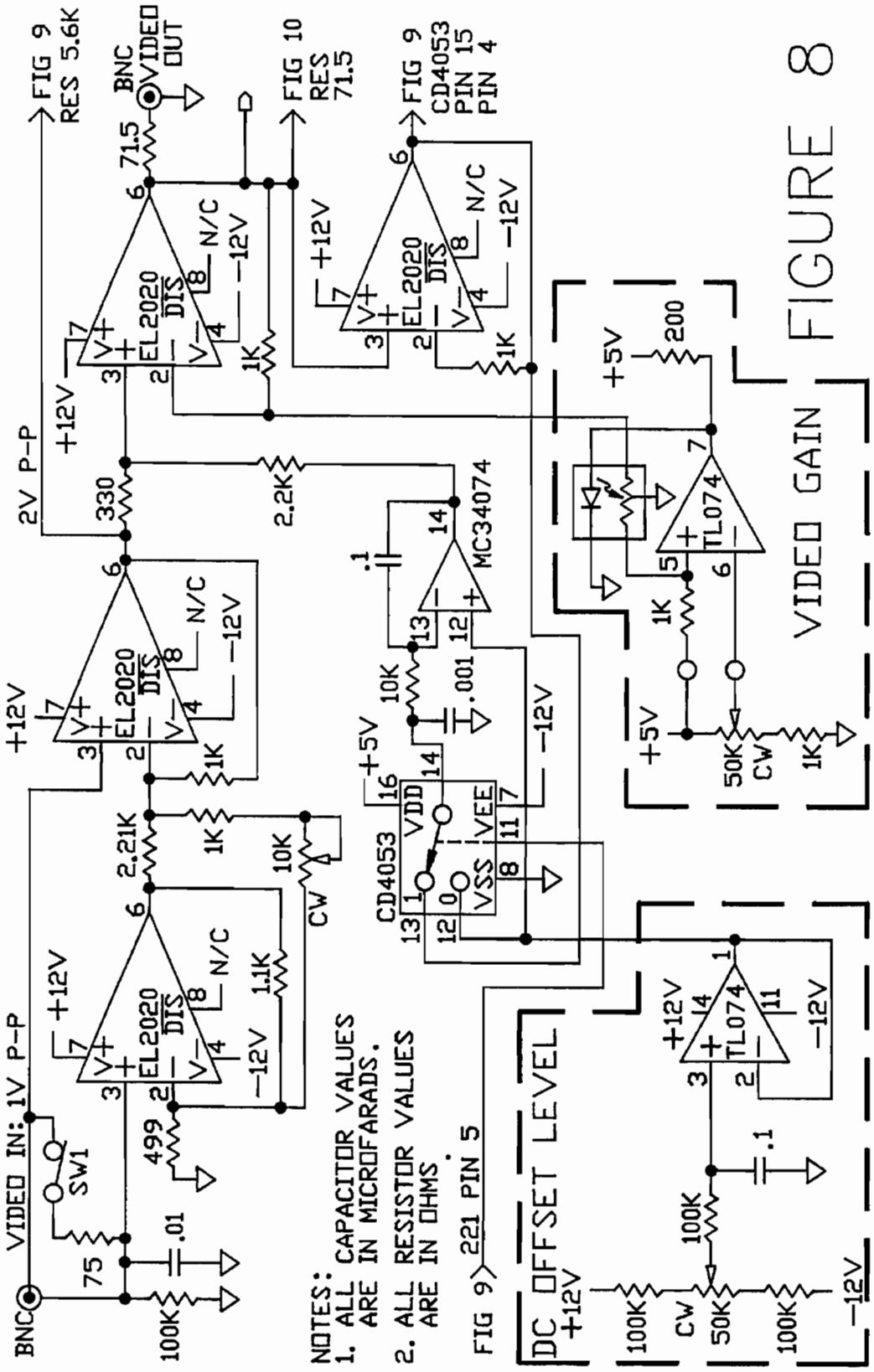


FIG 9 RES 5.6K
BNC VIDEO OUT
FIG 10 RES 71.5
FIG 9 CD4053 PIN 15 PIN 4
71.5
EL2020
+12V
-12V
N/C
1K
2V P-P
330
2.2K
MC34074
.1
10K
.001
+5V
CD4053
VDD
VSS
VEE
2.21K
1.1K
CW
499
.01
75
SW1
VIDEO IN: 1V P-P
BNC
100K
TL074
200
50K
VIDEO GAIN
DC OFFSET LEVEL
FIG 9 221 PIN 5
NOTES:
1. ALL CAPACITOR VALUES ARE IN MICROFARADS.
2. ALL RESISTOR VALUES ARE IN OHMS.

FIGURE 8

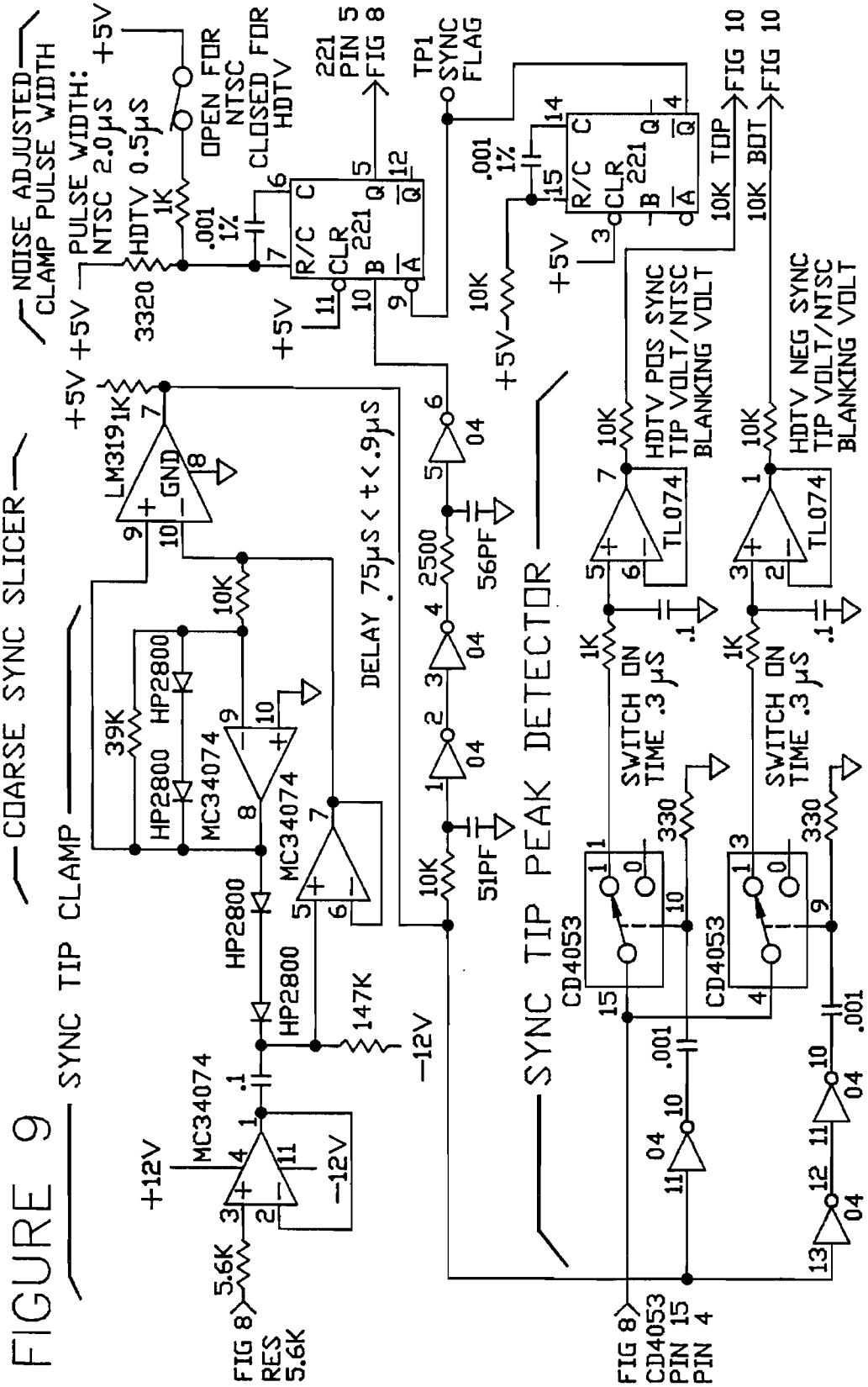

NOISE ADJUSTED CLAMP PULSE WIDTH
PULSE WIDTH: NTSC 2.0µS HDTV 0.5µS
+5V
OPEN FOR NTSC
CLOSED FOR HDTV
221 PIN 5 FIG 8
TP1 SYNC FLAG
3320
1K
.001 1%
R/C C CLR 221 B A Q Q
+5V
10K
LM319 GND
DELAY .75µS < t < .9µS
2500
56PF
51PF
04
COARSE SYNC SLICER
SYNC TIP CLAMP
39K
HP2800
MC34074
147K
-12V
+12V
.1
5.6K
FIG 8 RES 5.6K
SYNC TIP PEAK DETECTOR
HDTV POS SYNC TIP VOLT/NTSC BLANKING VOLT
HDTV NEG SYNC TIP VOLT/NTSC BLANKING VOLT
TL074
SWITCH ON TIME .3 µS
CD4053
330
.001
FIG 8 CD4053 PIN 15 PIN 4
10K TOP
10K BOT
FIG 10
FIG 10
FIGURE 9

FIGURE 10

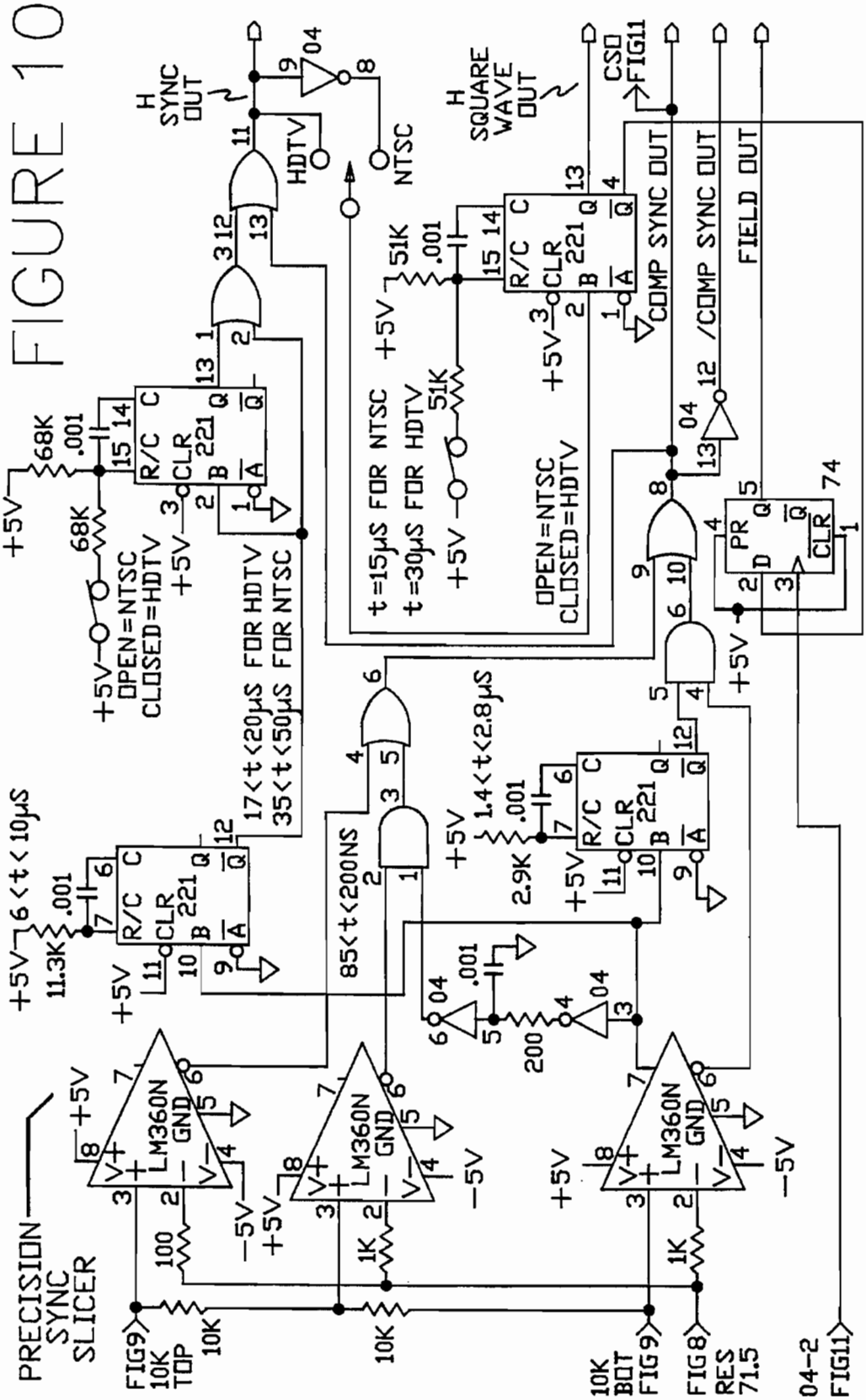
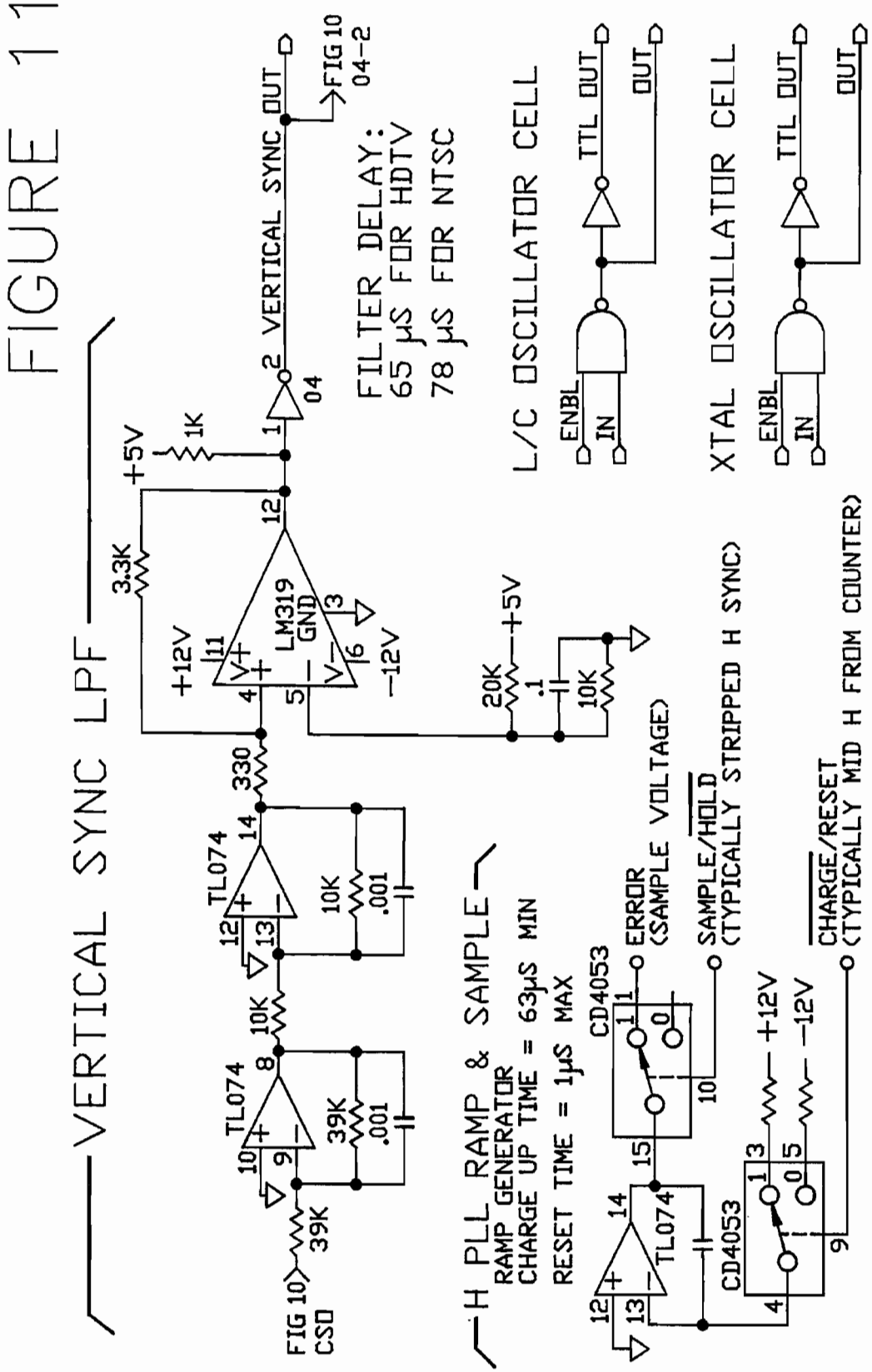

H SYNC OUT
HDTV
NTSC
H SQUARE WAVE OUT
CSO FIG11
COMP SYNC OUT
/COMP SYNC OUT
FIELD OUT
+5V
68K
.001
OPEN=NTSC CLOSED=HDTV
17<t<20µS FOR HDTV
35<t<50µS FOR NTSC
t=15µS FOR NTSC
t=30µS FOR HDTV
51K
OPEN=NTSC CLOSED=HDTV
6<t<10µS
11.3K
85<t<200NS
1.4<t<2.8µS
2.9K
200
LM360N
GND
100
1K
10K
-5V
PRECISION SYNC SLICER
FIG9 10K TOP
10K BOT FIG9
FIG8 RES 71.5
04-2 FIG11

FIGURE 11


VERTICAL SYNC LPF
+5V
1K
3.3K
+12V
LM319
GND
−12V
330
TL074
10K
.001
39K
FIG 10
CSD
2 VERTICAL SYNC OUT
FIG 10
04-2
FILTER DELAY:
65 µS FOR HDTV
78 µS FOR NTSC
L/C OSCILLATOR CELL
ENBL
IN
TTL OUT
OUT
XTAL OSCILLATOR CELL
H PLL RAMP & SAMPLE
RAMP GENERATOR
CHARGE UP TIME = 63µS MIN
RESET TIME = 1µS MAX
20K
.1
CD4053
ERROR
(SAMPLE VOLTAGE)
SAMPLE/HOLD
(TYPICALLY STRIPPED H SYNC)
CHARGE/RESET
(TYPICALLY MID H FROM COUNTER)

SYNCHRONIZING SIGNAL SEPARATING APPARATUS AND METHOD

This application is a continuation of application Ser. No. 07/837,323, filed Feb. 18, 1992, now abandoned.

BACKGROUND OF THE INVENTION

The present invention relates to signal processing systems and, in particularly, to video signal processing. A major objective of the present invention is a synchronizing signal processing apparatus and a method that precisely recovers synchronizing signals of a video signal.

Much of modern technology depends on signal processing. A common application of signal processing is for the video signal. Usually, a video signal includes picture synchronizing information. The synchronizing information is transmitted for scanning in a receiver in exact synchronism with a camera-tube scanning. The synchronizing signal must first be recovered from the video signal.

More particularly, TV (Television) video signals, the example of the video signal, are processed to obtain desired picture quality. A TV transmitting station modulates video and audio signals and transmits them out by an antenna so that TV receivers may receive them to produce the pictures. In order to precisely reproduce pictures, synchronizing information is added in the video signal so that the receivers can synchronously perform scanning operation as the TV transmitting station does.

Numerical and graphical criteria which describe essential aspects of a TV system, employed in the design and operation of equipment to assure that the various parts of the system will operate in cooperative fashion at maximum performance. TV systems have a special need, compared with other communication systems, for definitive standards because television transmitters and receivers must operate in a precise "lock-and-key" relationship. In particular, the scanning of the image in the camera must be matched by the scanning in every associated receiver within a timing precision of approximately one-tenth of a millionth of a second, and with relative positions of picture details correct to a few hundredths of an inch as viewed on the CRT or other display.

To assure that any television receiver can receive programs from any transmitter within range, it is customary to set up a single set of standards with a group of neighboring countries. The TV transmitting stations of different countries and areas transmit video signals with different formats. For example, U.S.A, Canada and Japan et al. use NTSC (National Television System Committee) system. France, Soviet Union et al. use SECAM (Sequential Couleura Memoire) system. Germany and United Kingdom et al. then use PAL (Phase Alternation Line) system. Moreover, HDTV (High Definition TV) creates a new system with images of high resolution. For all of these examples, the synchronizing signals added in their video signals are different.

Picture synchronizing information is obtained from the video signal by means of sync separation circuits. In addition, these circuits must separate this information from noise and interference during the reception of weak signals, particularly if impulse noise is present. To reproduce these different video signals of respective systems, different video signal processing devices are needed to provide required synchronizing signals.

Conventional video signal devices for processing the synchronizing information of the video signals can not be used for different standard video signals for providing

reliable synchronizing signals, without affecting the reproduction of the video signals or causing high cost of video signal processing. What is needed is a synchronizing signal processing apparatus and method that precisely recovers synchronizing signals of the video signal and can be applied for processing different video signals.

SUMMARY OF THE INVENTION

In accordance with the present invention, a synchronizing signal processing apparatus includes means for sampling synchronizing signals and slicing a video signal in response to the sampled synchronizing signals. The synchronizing signal processing apparatus includes a sampling means that samples the synchronizing signals and provides at least a reference signal. The synchronizing signal processing apparatus also includes a comparing means that slices the video signal in response to the at least a reference signal representing different levels of each of the synchronizing pulses. Thus, the synchronizing signal processing apparatus generates logic level outputs. The video signal with which the present invention is used may be of a standard type having synchronizing pulses including horizontal synchronizing pulses.

The video signal may be sliced, before it is sampled, to eliminate noise. The sliced video signal corresponds to the synchronizing pulses. In response to the sliced video signal, the peaks of the synchronizing pulses of the video signal are precisely sampled. Two sampled signals represent the positive and negative peaks of the synchronizing pulses. The two sampled signals further are divided into three reference signals to compare with the video signal. After this comparison, the logic outputs are combined to recover synchronizing pulses that are reliable, precise and without noise.

A combining means couples to the comparing means so that the outputs from the comparing means are combined depending on the type of the video signal. The combining means generates a plurality of synchronizing signals.

To provide a vertical synchronizing signal, the present invention uses a filtering means that filters one of synchronizing signals output from the combining to provide a vertical synchronizing signal. The filter means shows a good frequency response characteristic for the vertical synchronizing signal.

The synchronizing signal processing method in accordance with the present invention comprises steps of slicing a video signal sampling the video signal in response to respective leading and trailing edges of the sliced signal, converting the sampled signal into at least a reference signal, comparing the reference signal with the video signals and combining the compared outputs to recover synchronizing pulses.

An advantage of the synchronizing signal processing apparatus and method is that the present invention incorporates several standard functions with superior performance. The synchronizing signal processing apparatus in accordance with the present invention is capable of operating with standard two level synchronizing pulses, for example, NTSC, PAL and SECAM type synchronizing pulses, and three level synchronizing pulses, for example HDTV synchronizing pulses. The present invention may also applied for other video type signals with synchronizing pulses.

Furthermore, the present invention provides good bandwidth properties and time constant in the video amplifier section. The combination of the both proper bandwidth and time constant gives considerably noise immunity against

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United States Patent [19]

Cooper

[11] Patent Number: 5,486,869

[45] Date of Patent: Jan. 23, 1996

[54] **SYNCHRONIZING SIGNAL SEPARATING APPARATUS AND METHOD**

[76] Inventor: **J. Carl Cooper**, Twin Parks Bldg., 718 University Ave., Suite 210, Los Gatos, Calif. 95030

[21] Appl. No.: **165,688**

[22] Filed: **Dec. 13, 1993**

Related U.S. Application Data

[63] Continuation of Ser. No. 837,323, Feb. 18, 1992, abandoned.

[51] **Int. Cl.**[6] **H04N 5/08**

[52] **U.S. Cl.** **348/525**; 348/521

[58] **Field of Search** 348/525, 529, 348/530, 531, 521; 375/113; 307/351; H04N 5/08, 5/10

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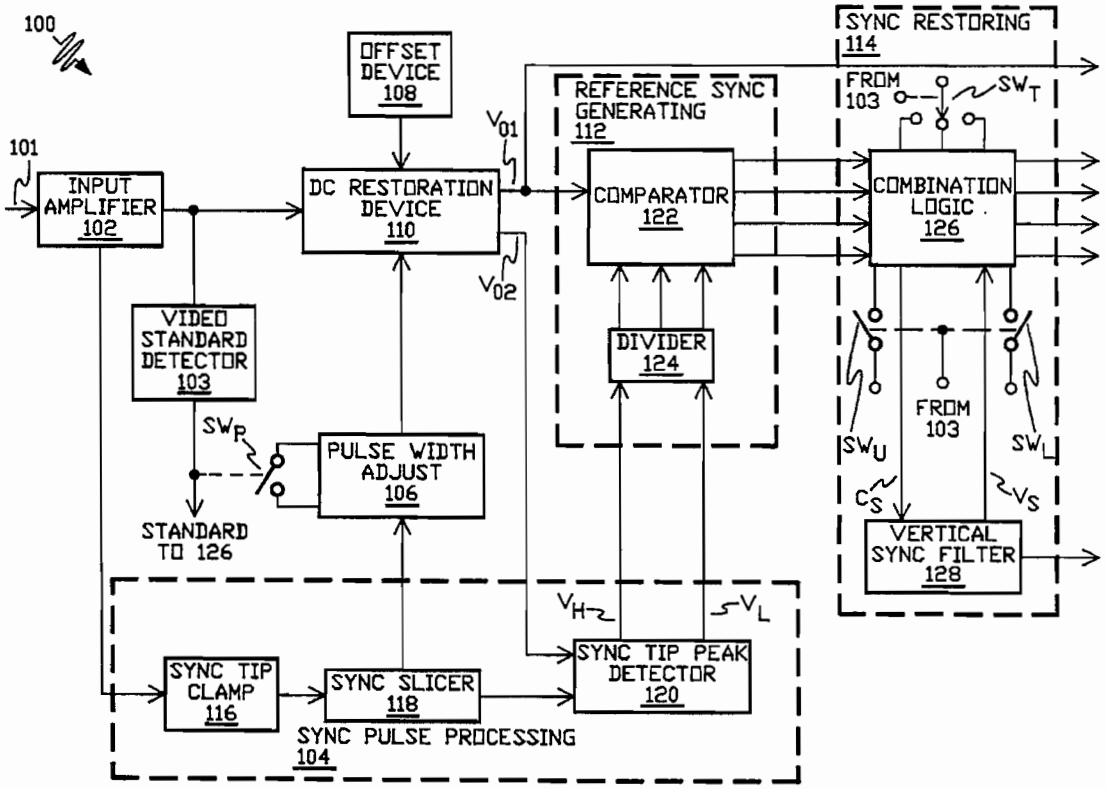
Primary Examiner—James J. Groody
Assistant Examiner—Chris Grant
Attorney, Agent, or Firm—J. Carl Cooper

[57] **ABSTRACT**

The present invention provides a synchronizing signal separation. In accordance with the present invention, a sync pulse processing circuitry slices a video signal and senses the peaks of the synchronizing pulse. A reference generating circuitry divides the output from the sync pulse processing circuitry into a plurality of reference signals that are compared with the video signal, thereby producing logic level outputs. A sync restoring circuitry combines the logic level outputs to provide precisely reconstructed synchronizing pulses of the video signal. The present invention incorporates different standard functions with superior performance because it may be applied for different types of video signals.

41 Claims, 11 Drawing Sheets



high frequency noise, yet maintains sufficient operation speed for high performance. Therefore, no additional compensation or filtering components are needed.

The synchronizing signal processing apparatus in accordance with the present invention may be easily adjusted for either two level or three level synchronizing pulses. The recovered synchronizing levels for video signals are characterized by high precision and reliability.

The logic level outputs of the comparing means are combined, the combination depending on whether the synchronizing pulses are two levels or three levels. In accordance with the present invention, the synchronizing signal processing apparatus may generate a TTL (Transistor-Transistor level) version of the synchronizing pulses.

The synchronizing signal processing apparatus in accordance with the present invention may be used with different video devices, which simplifies the design and manufacture of video devices, and significantly decreases the cost to make these video devices.

Another advantage of the synchronizing signal processing apparatus of the present invention is that it is suitable to be implemented by integrated circuits. Alternatively, the video signal processing can be implemented by software, such as in signal processing applications. These and other features and advantages of the present invention are apparent from the description below with reference to the following drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. **1** is a block diagram of a synchronizing signal processing apparatus in accordance with the present invention.

FIG. **2** illustrates a detailed circuit diagram of a sync pulse processing section of the synchronizing signal processing apparatus of FIG. **1**.

FIG. **3** illustrates a detailed circuit diagram including a pulse width adjust and a reference sync generating section of the synchronizing signal processing apparatus of FIG. **1**.

FIG. **4** illustrates a detailed circuit diagram of a sync restoring section of the synchronizing signal processing apparatus of FIG. **1**.

FIG. **5** shows waveform diagrams of several nodes of the synchronizing signal processing apparatus.

FIG. **6** shows a frequency response characteristic of a filter device of the synchronizing processing apparatus of FIG. **1**.

FIG. **7** is a flow chart of a synchronizing signal processing method in accordance with the present invention.

FIGS. **8–11** are four sheets of a detailed schematic of the preferred embodiment in accordance with the present invention.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

A synchronizing signal processing apparatus **100** in accordance with the present invention includes an input amplifier **102**, a video standard detector **103**, a sync pulse processing section **104**, a pulse width adjust **106**, an offset device **108**, a DC (Direct Current) restoration device **110**, a reference sync generating section **112** and a sync restoring section **114**.

Video signal **116** is applied to differential input amplifier **102** where video signal **101** is amplified to improve the ratio of signal/common mode noise. The video signal amplified by input amplifier **102** is fed to sync pulse processing section **104** which includes a sync tip clamp **116**, a sync slicer **118** and a sync tip peak **15** detector **120**.

The video signal is first clamped by sync tip clamp **116** to generate a clamped signal which has a known DC level of the synchronizing pulses. The clamped signal is then transferred to sync slicer **118** where the clamped signal is sliced, thereby generating a signal that has the same time period as that of the synchronizing pulses but at standard levels as compared to that of the synchronizing pulses, in this example TTL levels. To effectively eliminate interference and noise, the sync slicer **118** slices the synchronizing pulses at a known level which is preferred to be about half of the nominal expected amplitude of the synchronizing pulses. Due to the a known level which is approximately half the expected level, the operation of sync slicer **118** may be considered a coarse slicing operation which provides coarse sliced pulses. The sliced signal is coupled to sync tip peak detector **120**, in which peaks of synchronizing pulses of the video signal from DC restoration device **110** are sampled in response to the sliced signal.

The clamped signal is also delivered to pulse width adjust **106**. This clamped signal activates pulse width adjust **106** to generate a pulse trigger signal coupling to DC restoration device **110**. The pulse trigger signal determines the pulse width of the synchronizing pulses. A switch SW_P is provided with pulse width adjust **106**. Changing the status of the switch SW_P may adjust the width of the pulse trigger signal.

The video standard detector **103** is provided for determining the video signal output from the input amplifier **102**. When the video signal, for example, is a NTSC video signal, video standard detector **103** controls switch SW_L, so that this switch is open, which indicates that the video signal is a NTSC TV signal. On the other hand, when the video signal output from the input amplifier **102** is a HDTV signal, the video standard detector **103** will turn switch SW_P on. The video standard detector **103** also control switches SW_T, SW_U and SW_L. The switches may be operated automatically in response to a video standard detector **103** which detects the type of signal **101**. Therefore, the synchronizing signal processing apparatus **100** in accordance with the present invention may process different video signals.

Offset device **108** provides a DC reference for DC restoration **110**. The amplified video signal from the input amplifier **102** is also coupled to DC restoration **110**. In response to the reference from offset device **108**, DC restoration **110** clamps the amplified video signal to eliminate DC shift and residual common mode noise.

Other types of DC restoration circuits may be used as is well known in the art. It is desired to have the video signal V_{O1} and V_{O2} restored to a known value. However, it should be noted that the DC restoration device **110** may be eliminated by directly AC coupling the video signal output from the input amplifier **102** to the reference sync generating section **112** and sync pulse processing section **104**. The operation of sync tip peak detector **120** will track the variations in the AC coupled video signal output from the input amplifier **102** and allow the comparator **122** to function properly. However, the use of a DC restoration device is preferred.

The DC restoration device **110** produces two output signals V_{O1} and V_{O2}. The clamped video signal V_{O2} is delivered to sync tip peak detector **120**. In response to the sliced signal from the sync slicer **118**, sync tip peak detector **120** samples the positive and negative peaks of synchronizing pulses of the clamped video signal so as to provide two

peak sample pulse signals. For purpose of the present example, video is described with respect to positive white with the negative level of sync being that which is farthest from peak white video and the positive level of sync being that which is closest to the peak white value of the video. For two level sync, such as NTSC, the positive peak will correspond to video blanking level. The two peak sample pulse signals define each of synchronizing pulse. Divider **124** receives them and converts them into three pulse reference signals. The amplitudes of the pulse reference signals represent percentage levels of sync of V_{O2} during the respective ones of the peak sample pulses as represented by V_h and V_l.

Reference sync generating section **112** also includes a comparator **122**. The clamped video signal from DC restoration **110** and three pulse reference signals are coupled to comparator **122**. By comparation, comparator **122** outputs four level signals during each synchronizing pulse of the video signal. Due to the use of references which are responsive to the actual level of the sync pulse, the comparator **122** may be considered a precision comparator, which outputs precision sliced pulses. The four level signals represent different amplitudes of each synchronizing pulse as determined by the video sync being greater than none, one, two or three of the pulse reference signals.

A sync restoring section **114**, which includes combination logic **126** and vertical sync filter **128**, is arranged to receive the output signals from the comparator **122** of reference sync generating section **112**. The combination logic **126** is used to combine the four output signals from comparator **122** to recover reliable synchronizing signals. Switches SW_U and SW_L are arranged to control the switching between the HDTV video signal and conventional TV video signals, for example NTSC TV video signal.

The opening of switches SW_U and SW_L indicates that the synchronizing signal processing apparatus operates with conventional video signal. Otherwise, the closing of the switches SW_U and SW_L shows out that the apparatus operates with HDTV video signal. The position of another switch SW_T is also related to the video signal being processed by the apparatus in according with the present invention. Therefore, the apparatus of the present invention is suitable to different video signals by changing status of these switches, which may respond automatically to the video standard detector **103** as well.

The vertical sync filter **128** is coupled to the combination logic **126**. A composite synchronizing signal C_S from the combination logic **126** is coupled to it. The vertical sync filter **128** filters the composite synchronizing signal C_S to provide a vertical synchronizing signal V_S. The vertical sync filter **128** may respond to composite synchronizing signal from other sections as well, for example from **112**.

The sync pulse processing section **104** of synchronizing signal processing apparatus **100** is detailed with reference to FIG. **2**. Input amplifier **102** includes two operational amplifiers OP1 and OP2. OP1 is used with OP2 to eliminate common mode noise of the video signal **101**. The positive input of OP1 receives one of input video signal **101** which is the common one (shield) of the input signals. Resistor R1, 100 KΩ, is an input resistor for stabilizing the DC component of the input video signal.

A resistor R2 (75 Ω) and a switch SW_I are connected between the input lines for terminating video signal **101**. When the input is taken from other than the end of a coaxial cable run, SW_I is open. While the video signal **101** is applied to input amplifier **102** at the end of a coaxial cable run, SW_L is closed so that the input resistance of input amplifier **102** is matching the output resistance of the circuitry providing video signal **101**, thereby reducing signal loss. Capacitor C1 (0.1 μf) provides a high frequency bypass from the common to ground. R2 is the terminating resistor (75 Ω). OP1 and resistors R3 (1.10 kΩ) and R4 (499 Ωconstitute a negative feedback amplifier its gain being two approximately. The output of OP1 is coupled to the negative input of OP2 via resistor R5, 2.21 KΩ.

The positive input of OP2 receives the signal directly from the input signal **116**. OP2 and resistors R6, R7 and potentiometer R8 provide another feedback amplifier. Resistor R6 and R7 have the same resistance, 1.0 KΩ. The potentiometer R8 has a resistance from 0 –10 KΩ. Thus, the gain of the input amplifier **102** may be adjusted between 1.5–3. Due to the delay caused by OP1, the common mode component of signal **101** arrives at the positive and negative inputs of OP2 at slightly different moment. Under low frequency, the delay due to OP1 is tolerable. However, high frequency components of the input video signal, after delay by OP1, would severely affect correlation of the common mode signal, causing distortion of video signal. Therefore, a filter having capacitor C1 of 0.01 μf is utilized to filter the interference and noise to ground.

The output of OP2 is coupled to the sync tip clamp **116** of the sync pulse processing section **104**. The sync tip clamp **116** includes buffers OP3 and OP4, and an amplifier OP5. Resistor R9 (5.6 KΩ) is used with capacitor C2 to by-pass undesired frequency components. The buffered video signal is coupled to the positive input of another buffer OP4 via an isolating capacitor C3, 0.1 μf. A negative 12 V is applied to the isolating capacitor C3 and the positive input of OP4, via a current limit resistor R10, 147 KΩ. R10 effectively constitutes a constant current source. The isolating capacitor C3 is used to isolate the direct current components of the video signal.

The negative 12 V applied to the capacitor C3 draws node N1 toward a negative level, pulling the video signal output from OP3 to a negative level. The negative video signal, after buffering by buffer OP4, is coupled to the negative input of the amplifier OP5 via a resistor R11 with resistance of 10 KΩ. OP5 and a resistor R12 with resistance of 39 KΩ establishes a negative feedback amplifier. The positive input of OP5 is grounded. The resistance of the resistor R12 determines the maximum gain of amplifier OP5, which may be lowered if D3, D4 conduct.

Normally, the output of OP5 is negative. Two diodes D1 and D2 are provided to isolate the output of OP5 from the node N1. When the output of OP5 is above a level required to turn the D1 and D2 on, for example 1.2 V, the capacitor C3 is charged positive. The resistor R10 charges C3 negative, but is countered by the current through D1 and D2 when the video signal is below the ground of the positive input of OP5, thus causing N1 to move in a positive direction, which forces the output signal of OP5 to be returned to a negative value. The other two diodes D3 and D4 are arranged between the negative input and output of OP5. When the video signal at the negative input of OP5 is more positive by a level high enough to turn D3 and D4 on, the negative input and output of OP5 are shorted so that OP5 functions as a buffer and prevents large negative excursions at the output, thereby causing OP5 to recover to normal status very quickly, when returning positive.

Sync slicer **118** includes a comparator CP6. The output of OP5 is directed to the positive input of CP6. The output of OP4 is directed to the negative input of CP6. By comparison

of the signals at its inputs, CP6 slices the synchronizing pulses of the video signal at about half of the amplitude. By using both the outputs of OP4 and OP5, the comparison is less sensitive to noise and sync amplitude variations than if a fixed level were used. For the NTSC and HDTV video signals, the output of CP6 has a delay about 0.1 μs. Comparator CP6 slices the amplitude of the synchronizing pulses without appreciable change of pulse width.

The sliced pulses output from CP6 are directed to the sync tip peak detector **120**. The sync tip peak detector **120** includes sample switches SW_1 and SW_2, and two sample holders consisting resistors R15 and R16 with the same resistance of 1 KΩ, and capacitors C6 and C7 with the same capacitance of 0.1 μf. Resistor R15, capacitor C6 and switch SW_1 constitute a sample and hold circuit. Resistor R16 and capacitor C7 and SW_2 constitute another sample and hold circuit. Two buffers OP7 and OP8 are respectively coupled to the two sample and hold circuits to output the sampled signals.

The sliced pulses from CP6 are first inverted by an invertor I1. Thus, the rising edge of the inverted pulses coincide with the trailing edge of the output pulses of CP6. Each of the inverted pulses is then differentiated at its rising edges, by means of a differential capacitor C4 of 0.001 μf and a differential resistor R13 of 330Ω. The switch SW_1 is in the receipt of the signal V_{O2} output from the DC restoration device **110**. Usually, switch SW_1 is tied to ground via resistor R13. Only upon the arrival of the rising edges of the inverted pulses, switch SW_1 is activated to couple to the hold circuit having R15 and C6. Therefore, corresponding to each falling edge of the sliced pulses output from CP6, R15 and C6 sample the positive peaks of the pulses. Note that the sliced sync from CP6 is opposite in polarity to the sync of V_{O2}. The sampled positive peak is held for the buffer OP7 to output. The width of differential pulse for sampling the video signal is set by C4 and R13.

Similarly, after inversion twice by invertors I2 and I3, the output of CP6 is differentiated by a differential capacitor C5 of 0.001 μf and a different resistor R14 of 330Ω. Thus a differential pulse is coupled to switch SW_2. The differential pulses produced by C5 and R14 cause the switch SW_2 close so that a resistor R16 of 1 KΩ and a capacitor C7 of 0.1 μf hold the negative peaks of the synchronizing pulses. The two signals which operate sample switches SW1 and SW2 can be described as reference taking signals, since they take the instant samples which are in turn held by the hold capacitors to generate the voltage reference signals used by the divider **124** to provide reference for comparator **122**.

As a result, each of the pair of differential pulses produced by C4, R13, C5 and R14 defines the pulse position of respective synchronizing pulses. The relationship of the output pulses of CP6 and the differential pulses is shown in FIG. **5**. Furthermore, buffers OP7 and OP8 deliver the peak sample signals to divider **124** for further processing.

The video signal amplified by the input amplifier **102** is also coupled to the DC restoration device **110**, referring to FIG. **3**. The DC restoration device **110** includes a voltage comparator CP9, a photosensitive element having a LED (light-emitting diode) D_u and a photoresistor R59, an amplifiers OP10 and a buffer OP11. A positive 5 V DC voltage is tied to a resistor R17 of 1.0 KΩ, the left part of the photoresistor R59 and the tap of R16 is connected to ground. Thus, the voltage applied to the positive input of the CP9 depends on the resistance of left part of R59. On the other hand, the positive 5 V is tied to a series connection of potentiometer R18 and a resistor R19 and to ground. Thus, the reference voltage at the negative input of CP9 is defined by the position of the wiper of potentiometer R18. Therefore, adjusting the position of the wiper of potentiometer R18 may change the input voltage at the negative input of CP9.

At the output of CP9, a positive 5 V is applied to the LED Du through a resistor R20 of 200Ω. The positive 5 V provides an offset current to LED D_u. The light intensity of the LED Du is in proportion to the current flowing through it. The resistance of photoresistor R59 is inversely proportional to the light intensity. Therefore, the higher the output of CP9, the larger the current through the LED Du, the lower the resistance of the photoresistor R59. The lower resistance of R59 makes the voltage applied to the positive input of CP9 go down, thereby causing the output of CP9 to decrease. CP9 thus causes R59 to maintain the voltage at the positive and negative inputs of CP9 to be equal.

The output of the input amplifier **102** is coupled to the positive input of the amplifier OP10 of DC restoration **110**, via a resistor R1 of 330Ω. The output of OP10 is tied to the negative input via a feedback resistor R22, 1.0 KΩ and the right part of the photoresistor R59 ties the negative input of OP10 to ground. Because the output of CP9 may change the resistance of R59, the gain of OP10 is also controlled by the output of CP9. Therefore, changing the position of the wiper of potentiometer R18 changes the gain of OP10.

The output of OP10 is applied to the positive input of amplifier OP11. Along with a resistor R23 of 1.0 KΩ, the operational amplifier OP11 buffers the output of OP10. The video signal from buffer OP11 is transferred to the sync tip peak detector **120** where the video signal is sampled in response to the pulses from the sync slicer **118**, as shown in FIG. **2**. The video signal output amplified by OP10 is also sent out by an output resistor R24, 71.5Ω for other purposes.

An offset device **108** is arranged to provide a DC offset required by the operational amplifier OP13 of the DC restoration **110**. The offset device **108** includes a resistor network having a resistor R57 (100 KΩ), a resistor R57 (100 Ω) and a potentiometer R55. A positive 12 V is coupled to resistor R57 and a negative 12 V is coupled to resistor R25. A voltage determined by the position of the wiper of potentiometer R55 charges a capacitor of 0.1 μf via a resistor R58 of 100 KΩ. The level on the capacitor C13 is applied to the positive input of a buffer OP12.

The offset voltage is delivered to an integrator circuit established by a operational amplifier OP **13** and a capacitor C8 (0.1 μf) bridging between the negative input and output of OP13. The positive input of OP13 receives the offset voltage. The offset voltage is also coupled to a switch SW_3. The common close status of SW_3 couples the offset voltage to the negative input of OP13 via a resistor R25 of 10 KΩ. A capacitor C9 of 0.001 μf is tied between ground and SW_3 for filtering undesired frequency components and switching transients.

In accordance with the present invention, the pulse width adjust **106** is provided for. The pulse width adjust **106** includes two multivibrators **301** and **302**. The output from the sync slicer **118** is coupled to the A input of **301**, as shown in FIG. **3**. A positive 5 V, is tied to the clear input $\overline{Clr}$ of **301**. Responding to each falling edge of the sliced signal from sync slicer **118**, the multivibrator **301** produces a low level pulse at the $\overline{Q}$ output of **301**. The width of the low level pulse is set by a resistor R54 of 10 KΩ and a capacitor C10 of 0.001 μf. The output from **301** is shown in FIG. **5**.

The output from sync slicer **118** is also coupled to the B input of multivibrator **302** via a delay circuit. This delay

circuit includes two RC filters. A capacitor C14 (51 pf) and a resistor R28 (10 KΩ) form a RC filter and a capacitor C12 (56 pf) and a resistor R60 (2.5 KΩ) provide another one. Two invertors I4 and I5 are arranged between the two RC filters. An invertor I6 is positioned between the B input of 302 and RC filter having C12 and R60. A positive 5 V is applied to R28 via a resistor R58 (1kΩ) for providing a DC bias. This delay circuit delays the sliced signal from sync slicer 118 about 0.75 μs to 0.9 μs.

The pulses at the $\overline{Q}$ output of 301 trigger the multivibrator 302 via its $\overline{A}$ input so that the Q output of 302 is at high level. The delayed pulses by the delay circuit is applied to B input of 302, triggering it so that the Q output of 302 is at a high level. The pulse width of output pulse from 302 is set by a resistor R29 of 3.32 KΩ and a capacitor C11 of 0.001 μf, if the apparatus 100 in accordance with the present invention operates under conventional TV video signal mode, for example, the NTSC video signal. When the apparatus 100 operates under the HDTV mode, a resistor R30 of 1 KΩ is shunted with R29 by closing of the switch SW_P.

Therefore, the pulse width of Q output of 302 is between 2 μs and 2.5 μs for the NTSC video signal. This pulse occurs during blanking and burst portion of the NTSC video signal. On the other hand, the pulse width of the Q output of 302, for the HDTV video signal, is from 0.5 μs to 0.7 μs. The pulse of Q output of 302 coincides with the blanking portion without exceeding it. The waveform at the Q output of 301 is shown in FIG. 5.

The output pulses at the Q output of 302 activate the SW_3 so that the output from OP11 is coupled to the negative input of OP13 via the RC filter having the resistor R25 and the capacitor C9. During the high level of the pulses from 302, the capacitor C8 of the integrator OP13 is charged up and down by the video signal from the buffer OP11 depending on whether it is above or below the reference on the plus input of OP13, drawing the input voltage at the positive input of OP10 up or down. As a result, the output of OP10 is drawn or down. After the Q output of 302 recovers to low level, the switch SW_3 is released so that the negative input of the operational amplifier OP13 is coupled to the output of OP12 of the offset device 108. Thus, the 10 output of the operational amplifier OP13 does not change.

The divider 124 of the reference sync generating section 112 includes four resistors R31, R32, R33 and R34. The resistors R31–R34 have the same resistance of 10 KΩ. Therefore, the output potential of the sync tip peak detector 120 is equally divided so that three reference potentials are provided. The first reference potential between the resistors R33 and R34 equals half of the output potential from the sync tip peak detector 120. The second reference potential between the resistors R31 and R33 equals three-fourth of the output level from the sync tip peak detector 120. The third reference potential between the resistors R32 and R34 equals one-fourth of the output level from the sync tip peak detector 120. However, different reference potentials may also be obtained by changing the resistance of resistors R31–R34. Different combination of potentials on the positive inputs of CP14–CP16 can be easily realized.

In accordance with the present invention, the comparator 122 of reference sync generating section 112 includes three comparators CP14, CP15 and CP16. The first reference potential between the resistors R33 and R34 is applied to the positive input of comparator CP14. The second reference potential between the resistors R31 and R33 is applied to the positive input of the comparator CP15 The third reference potential is then applied to the positive input of the comparator CP16. The video signal output V_{O1} from the amplifier OP10 of the DC restoration 110 is coupled to respective negative inputs of three comparators CP14–CP16 via resistor R35, R36 and R37.

As for conventional TV video signals, for example, the NTSC video signal, CP14 compares the first reference potential and the video signal V_{O1} so as to sense the middle levels of the horizontal and vertical synchronizing pulses. The comparator CP15 then senses the video signal V_{O1} in response to the second reference potential and the rest of the video signal V_{O1} is regarded as noise. Because the switch SW_1 of sync tip peak detector 120 closes during the blanking-burst period to sample the video signal, the second reference potential is set to a level lower than the blanking level. The switch SW_2 of sync tip peak detector 120 closes during the negative synchronizing tip to sample the video signal, the third reference potential is thus set to a level higher than the negative tip. Two complementary outputs V_{P3} and V_{C3} from CP16 are delivered to the combination logic 126.

As a second example, when the apparatus 100 in accordance with the present invention is used for processing the HDTV video signal, the second reference potential represents a value between the blanking and positive peak synchronizing tip for the synchronizing pulses. The rest of the video signal V_{O1} is considered as noise. The first reference potential is set at the middle of the negative and positive synchronizing tip during synchronizing pulses, meaning at the blanking level. The purpose of this comparator CP14 is to sense transition from the negative synchronizing tip to the positive synchronizing tip. The rest of the video signal V_{O1} is considered as noise. The reference potential and the output V_{P3} of CP16 is the same as under the NTSC video signal. Therefore, outputs of comparator 122 are logic levels corresponding to the negative sync for these video signals.

The logic level outputs V_{P1}, V_{P2}, V_{P3} and V_{C3} from the comparator 122 are directed to the combination logic 126 of the sync restoring section 114, as shown in FIG. 4. The output V_{P1} of the comparator CP14 is directed to an input of an AND gate A1. The signal V_{C3} output from the comparator CP16 is inverted by an invertor I7, and is filtered by a RC filer having a resistor R53 (200Ω) and a capacitor C17 (0.001 μf). Before it is applied to another input of the AND gate A1, the filter signal V_{C3} is inverted again by an invertor I8. In order to preserve the combination logic generated sync information at the half way crossing, the output V_{C3} from the comparator CP16 is delayed by the invertor I7 and I8 circuit for 85 ns–200 ns. Thus, the two input pulses are anded at the inputs of the AND gate A1 so that the output of A1 is a positive pulse.

Along with the output from the AND gate A1, the output V_{P2} from the comaparator CP15 is directed to an input of an OR gate O1. The positive pulse from A1 and the V_{P2} activate the OR gate O1, thereby producing a pulse which has a rising edge defined by the positive pulse from A1 and a falling edge defined by V_{P2}. The output of OR gate O1 is directed to another OR gate O2.

The output V_{C3} is also used to trigger a multivibrator 401 so that a high level is set at the $\overline{Q}$ output of the multivibrator 401. The width of high level is set by a resistor R38 and a capacitor C8. In this case of capacitor C8 has a capacitance of 0.001 μf and resistor R38 has a resistance of 2.9 KΩ, the pulse width is between 1.4 μs–2.8 μs. The output high level at the $\overline{Q}$ output of 401 is directed to an input of an AND gate 35 A2. The another input of A2 receives the output V_{P3} from

the comparator CP16. For the NTSC video signal, the output of A2 is determined by signal V_{P3}. Under the HDTV video signal, the output of A2 is determined by the pulse at the $\overline{Q}$ output of 401. The minimum width for this pulse is 2.6 μs which determined by the duration of the vertical interval pulses. The maximum width for this pulse is 2.8 μs which is determined by the duration of the blanking in horizontal lines.

The ANDed output from A2 is applied to another input of OR gate O2 so that the output from OR gate O1 is ORed with the ANDed output from A2. Particularly, under processing the NTSC video signal, the ORed output of OR gate O1 is completely determined by the ANDed output pulse from A2. The reason is that the negative ANDed output from A2 is narrower than the negative ORed output from O1. The output of O2 is a composite synchronizing output C_S.

In order to extract horizontal synchronizing pulses from the output C_S from the OR gate O2, a circuitry including multivibrators 402 and 403, and OR gates O3 and O4 is designed. This circuitry eliminates every second half horizontal pulse from the vertical interval. The signal V_{C3} output from the comparator CP16 is directed to the multivibrator 402, where V_{C3} triggers the B input of 402 to set a low level at its $\overline{Q}$ output. The width of this low level is set by a capacitor C19 (0.001 μf) and a resistor R39 (11.3 KΩ). In this case, the low level lasts 6–10 μs. The 6 μs lower time limit is chosen to be greater than the horizontal synchronizing pulse duration. The upper time limit is chosen so that the pulse will not to get into active video signal.

The $\overline{Q}$ output of 402 triggers the B input of the multivibrator 403 so as to set a high level output at its Q output. The duration of the high level at the Q output of 403 is determined by a capacitor C20 (0.001 μf) and the combination of resistors R40 (68 KΩ) and R41 (50 KΩ). The position of switch SW_U is determined by the operation mode. For example, under the NTSC video signal, SW_U is open so that the duration of the high level at the Q output of 403 is set by R40 and C12, for example 35 μs–50 μs. On the other hand, if the apparatus 100 of the present invention is for processing the HDTV video signal, the switch SW_U is closed so that R41 is shunted across R40. Accordingly, the duration of the high level at the Q output of 403 is determined by C20 and the shunted resistors R40 and R41, for example 17 μs–20 μs.

The Q output of 403, along with the $\overline{Q}$ output of 402, is coupled to inputs of an OR gate O3. The output of OR gate O3 is the OR of the outputs of the both multivibrators 402 and 403. This output of O3 coincides with the synchronizing tip but lasts a little longer. The output of 03 is directed to an OR gate O4. Another input of the OR gate O4 receives the output from the OR gate O2. The OR gate O4 serves to eliminate the half horizontal pulses during the vertical intervals, thereby producing a horizontal synchronizing output H_S.

A multivibrator 404 is used to generate a horizontal square waveform output H_Q. The output H_S of the OR gate O4 is coupled to the B input of 404 via the switch SW_T. When the apparatus 100 of the present invention operates under the HDTV video signal, the rising edges of output H_S triggers 404 at the B input to set a high level output at its $\overline{Q}$ output. Meanwhile, the switch SW_L is closed so that the positive 5 V is applied to 404 via shunted resistors R42 and R43 and a capacitor C21. Accordingly, the duration of the high level depends on a capacitor C21 and the resistance of shunted resistors R42 and R43. If the capacitance of C21 is set as 0.001 μf and R42 and R43 are respectively set as 51 KΩ, the duration is then 30 μs.

If the apparatus 100 of the present invention operates with the NTSC video signal, the output H_S is reversed by an invertor I6 so that the B input of 404 is triggered by the falling edges of the synchronizing pulse, setting a high level at its Q output. At the same time, the switch SW_L is open so that the positive 5 V voltage is applied to 404 via only a resistor R42. Assuming R42 has the resistance of 51 KΩ and C31 has the capacitance of 0.001 μf, the duration of the high level at the Q output of 404 is 30 μs.

The output C_S of OR gate O2 is also directed to a vertical synchronizing filter circuitry including operational amplifiers OP17 and OP18. A resistor R44 of 37.4 KΩ and a capacitor C22 of 0.001 μf bridge across the output and negative input of OP17 to form a first stage low pass filter. The positive input of OP17 is tied to ground. The composite synchronizing output C_S is coupled to the negative input of OP17 via a resistor R52 of 39 KΩ. The output from OP17 is coupled to the negative input of OP18 via a 10 Ω resistor. The positive input of OP18 is tied to ground. A resistor R45 (10 KΩ) and a capacitor C15 (0.001 μf) are shunted across the negative input and the output of OP18, thereby providing a second stage low pass filter.

This vertical filter circuitry employs a design 25 offsetting conventional optimal design. This design provides a frequency response characteristic without matching standard filter design curves which are commonly known. However, it is this design that provides a frequency response characteristic good for vertical synchronizing separation of the NTSC or HDTV video signal. This frequency response of the filter circuitry is shown in FIG. 6.

The filtered signal is applied to a positive input of a comparator CP19 via a 330Ω resistor. A resistor R46 of 3.3 kΩ is bridged between the positive input and output of CP19 to provide positive feedback hysteresis for CP19. A positive 5 V voltage is tied to ground via resistors R47 and R48. R47 has resistance of 20 KΩ and R48 has resistance of 10 KΩ. A capacitor C16 of 0.1 μf is shunted across resistor R48, thereby providing a stable reference voltage to the negative input of CP19. Furthermore, a positive 5 V voltage is applied to the output of CP19 via a resistor R49 (1 KΩ). Filter circuitry provides a vertical synchronizing output V_S via CP19 and inverted by an invertor I10.

To obtain a field synchronizing output, the vertical synchronizing output from CP19 is directed to a flip-flop 405. The clear input CLR and set input PR of 405 are coupled to a positive 5 V. The CK input of 405 receives vertical sync and the D input of 405 is coupled to H sync square waveform the $\overline{Q}$ output of multivibrator 404. The rising edges of the V_S pulses activate the trigger 405 to produce the field synchronizing output F_S. Upon arrival of the rising edges, the Q output of 405 is set to such a level that is same as that at its D input. In addition, an invertor I11 is provided for outputting a reversed composite synchronizing output $\overline{C}_S$.

A processing method 700 for synchronizing pulses of the video signals is shown in FIG. 7. At step 701, the video signal is sliced to produce synchronizing pulses. The video signal is then sampled in response to the sliced sync to precisely sense the sync tip peaks pulses, at step 702, thereby providing two peak signal values representing the positive and negative peak values of each synchronizing pulse.

The peak signal values are further converted, at step 703, into three reference signals which respectively represent the different levels relative to each synchronizing pulse. In particular, the three reference levels respectively represent the middle, upper and lower middle levels of the synchronizing pulse. Comparison of the three reference levels and

the video signal is conducted at step **704**. As a result of this comparison, the logic pulse outputs are obtained. Step **705** is for restoring synchronizing pulses of the video signal by combining the logic outputs.

FIGS. **8–11** show a more detailed schematic circuit of a preferred embodiment in accordance with the present invention. All of the components in FIGS. **8–11** correspond directly to those presented in FIGS. **2–4**. The differences between FIGS. **2–4** and **8–11** are that all of components in FIGS. **8–11** are marked with commercial identification and are therefore more available in market. Therefore, detailed product part numbers and nominal values of components are marked on the components of FIGS. **8–11**. The operation principle and interconnection of the components of the circuitry shown in FIGS. **8–11** are corresponding to FIG. **1** and FIGS. **2–4** and one skilled in the art will be able to understand FIGS. **8–11** from the forgoing description and explanation. Thus, the description of FIGS. **8–11** is omitted here.

One skilled in the art will recognize that the above described functions and components are somewhat more complex than represented by the present block diagrams, however from the disclosure and teachings herein, taken with the available applications literature available from the manufacturers of the suggested components, or from other components which may be substituted as will be known from the above disclosure, the construction of a practical and operatable device will be well within the capability of one or ordinary skill in the art without resorting to further invention or undue experimentation.

It will be understood that the previous descriptions and explanations are given by way of example, and that numerous changes in the combinations of elements and functions as well as changes in design of the above may be made without departing from the spirit and scope of the invention as hereinafter claimed. In particular, it will be useful to combine the functions of the invention with other functions in a fashion so that such functions may be shared between devices or methods. These and other modification to and variations upon the embodiments described above are provided for by the present invention, the scope of which is limited only by the following claims.

What is claimed is:

1. A video signal processing apparatus for use with the synchronizing pulses thereof, said synchronizing pulses having at least a leading edge and a trailing edge including in combination:

at least one sampling circuit for sampling said synchronizing pulses in response to a plurality of sampling signals to generate at least a first reference signal and a second reference signal, said reference signals respectively representing different levels of said synchronizing pulses, wherein said sampling circuit includes DC restoring for restoring said synchronizing pulses to a predetermined DC reference level which said DC restored synchronizing pulses are coupled to at least one comparing circuit for comparing said video signal with a level responding to said reference signals thereby providing at least a precision sliced pulse signal, with said sampling being independent of said precision sliced pulse signal.

2. A video signal processing apparatus as recited in claim **1** wherein said sampling circuit further comprises:

a detecting circuit for detecting respective levels of said synchronizing pulses in response to said leading and trailing edges and outputting a first level signal and a second level signal; and

converting circuit for converting said first and second level signals into said first and second reference signals.

3. A video signal processing apparatus as recited in claim **2** wherein said first reference signal represents a middle level value of said synchronizing pulse, said second reference signal represents a level value above said middle level value, said sampling means further generates a third reference signal representing a level value below said middle level value.

4. A video signal processing apparatus for use with synchronizing pulses of a video signal including:

at least one sampling circuit for sampling said synchronizing pulses in response to a plurality of sampling signals provided , in response to said synchronizing pulses to generate at least a first reference signal and a second reference signal, said reference signals respectively representing different levels of said synchronizing pulses; and

comparing circuit for comparing said synchronizing pulses with a level responding to said reference signals to generate precision sliced pulses, with said sampling being independent of said precision sliced pulses, and further comprising combining said precision sliced pulses to generate horizontal rate and vertical rate pulse signals.

5. A video signal processing apparatus as recited in claim **4** wherein said combining comprises filtering for filtering one of said precision sliced pulse signals to generate said vertical rate pulse signal.

6. A synchronous signal processing apparatus for a video signal comprising:

slicing means for slicing said video signal to generate sliced pulses, said sliced pulses corresponding to respective synchronous pulses of said video signal, each of said sliced pulses having a leading edge and a trailing edge;

level detecting means for detecting respective levels of said synchronous pulses of said video signal in response to said leading and trailing edges and providing a first level signal in response to one of said edges and a second level signal in response to the other of said edges; and

sync restoring means for detecting different levels of said synchronous pulses in response to said first and second level signals and generating a derived sync pulse output in response thereto.

7. A synchronous signal processing apparatus as recited in claim **6** wherein said sync restoring means comprises:

transforming means for transforming said first and second level signals into a first reference signal, a second reference signal and a third reference signal; and

comparing means for comparing said synchronous pulses with said first, second and third reference signals to generate logic level outputs.

8. A synchronous signal processing apparatus as recited in claim **7** wherein said sync restoring means further comprises means for filtering said derived sync pulse output to generate a vertical synchronous output.

9. A synchronous signal processing apparatus as recited in claim **8** wherein said filter means operates in response to a frequency ranging from 0–10 KHz.

10. A synchronous signal processing apparatus as recited in claim **6** further comprising format selecting means for selecting the format of said video signal being processed.

11. A synchronous signal processing apparatus as recited in claim **6** wherein said first and second level signals

respectively represent a positive peak value and a negative peak value of said synchronous pulses.

12. A synchronous signal processing apparatus as recited in claim **8** wherein said filter means substantially operates to pass frequencies ranging from 0–1 KHz with less than 50% normalized amplitude attenuation, and having at least 90% normalized amplitude attenuation at frequencies greater than 10 KHz said normalized attenuations with respect to the level of DC response at the output.

13. A video signal processing apparatus, said video signal having synchronous pulses of a pulse amplitude, said apparatus comprising:

sync tip clamping means for clamping said video signal to provide a clamped pulse signal, respective pulse of said clamped pulse signal having a leading edge and a trailing edge;

peak detecting means for sampling said video signal in response to said leading and trailing edges to generate a positive peak signal and a negative peak signal;

level dividing means for dividing level between said positive and negative peak signals into a first reference level, a second reference level and a third reference level; and

comparing means for comparing said video signal with respective said reference levels to generate logic level outputs.

14. A video signal processing apparatus as recited in claim **13** wherein said first reference level represents a mean value of said pulse amplitude, said second reference level represents a upper value and said third reference level represents a lower value.

15. A video signal processing apparatus as recited in claim **14** wherein said upper value is a sum of said mean value and an offset value, said lower value is a difference of said mean value and said offset value.

16. A video signal processing apparatus as recited in claim **15** wherein said offset value is one half of the value between said mean value and said positive peak.

17. A video signal processing apparatus, said video signal having synchronous pulses of a pulse amplitude, said apparatus comprising:

format selecting means responsive to the format of said video signal for determining the format of said video signal being processed;

sync tip clamping means for clamping respective sync tips of said video signal to provide a clamped pulse signal corresponding to said synchronous pulses, each respective pulse of said clamped pulse signal having a leading edge and a trailing edge;

sync slicing means coupling to said sync tip clamping means, for limiting an amplitude of said clamped pulse signal to provide a coarse sliced sync signal;

peak detecting means for sampling positive and negative peaks respectively of said synchronous pulses of said video signal in response to said leading and trailing edges, thereby generating a positive peak signal and a negative peak signal;

level dividing means for dividing level between said positive and negative peak signals into a first reference level, a second reference level and a third reference level, said first, second and third reference levels respectively representing different portion levels of said pulse amplitude;

comparing means for comparing said video signal with respective said reference levels to generate logic level outputs; and

restoring means coupling to said comparing means, for combining said logic level outputs to generate a plurality of precision synchronous outputs.

18. A video signal processing apparatus as recited in claim **17** wherein said first reference level represents a mean value of said pulse amplitude, said second reference level represents a level value above said mean value and said third reference level represents a value below said mean value.

19. A method for processing a synchronous signal of a video signal comprising steps of:

slicing said video signal to generate a sliced sync pulse signal;

sampling said video signal in response to respective leading edges and trailing edges of said sliced pulse signal so as to generate a first sample level signal and a second sample level signal; converting said first and second sample level signals into a first reference signal, a second reference signal and a third reference signal, said first reference signal representing a middle level of each synchronous pulse of said video signal, said second reference signal representing a upper level above said middle level and said third reference signal representing a lower level below said middle level;

comparing said respective reference signals with said video signal to generate logic level outputs; and restoring desired synchronous pulses in response to said logic level outputs.

20. A video signal processing apparatus as recited in claim **19** wherein said method further comprises a step of adjusting a pulse width of said sliced sync pulse signal in response to a format selecting signal generated by a mode selecting switch.

21. A method of generating an output sync signal corresponding to the sync portion of a composite video signal which sync portion comprises a plurality of sync levels, one of which said sync levels includes blanking level, said method including the steps of:

a. generating a plurality of level signals having magnitudes responsive to said sync levels,

b. establishing at least one reference level between each of said sync levels in response to said level signals, the number thereof changeable in response to the number of said sync levels,

c. for each said reference level established, generating a binary pulse version of said sync portion by comparison of said reference levels and said sync portion,

d. generating said output sync signal in response to said binary pulse versions of step c.

22. A method of generating an output sync signal corresponding to the sync portion of a composite video signal which sync portion comprises a plurality of sync tip levels and a blanking level, said method including:

a. generating a plurality of level signals having magnitudes responsive to said sync tip levels,

b. establishing a plurality of reference levels between said sync tip levels in response to said level signals,

c. generating a plurality of binary pulse versions of said sync portion by comparison of said reference levels and said sync portion,

d. combining said plurality of binary pulse versions to generate said output sync signal.

23. A method as claimed in claim **21** or **22** wherein said sync portion takes on three or more levels including the blanking level and two or more reference levels are established such that their values lie substantially equidistant from the outer level signals.

24. A method as claimed in claim 21 or 22 wherein, said comparison of said reference levels and said sync portion provides time sequential binary pulse versions as said sync portion transcends said reference levels.

25. A method as claimed in claim 21 or 22 wherein said binary pulse versions are time sequential and are combined so that a first edge of said output sync signal occurs in response to a first said binary pulse version, and a second edge of said output sync signal occurs in response to a second said binary pulse version.

26. A method as claimed in claim 21 or 22 including the step of determining if said composite video signal is a HDTV type video signal, and modifying said reference levels in response thereto.

27. An apparatus for deriving a logic level version of the sync portion of a video type signal, said sync portion having a plurality of levels, one of which may be a blanking level, said apparatus including:

circuitry responsive to said sync portion to clamp the sync tip thereof to a known level thereby providing a clamped sync portion and to generate at least a first logic level sync signal in response to said clamped sync portion;

circuitry for clamping said sync portion to a known level to provide a second clamped sync portion;

circuitry for providing at least one reference signal in response to said first logic level sync signal and said second clamped sync portion;

circuitry for comparing said second clamped sync portion to said reference signal to provide said logic level version.

28. An apparatus as claimed in claim 27 wherein in said circuitry for clamping the sync tip to a known level, said known level is established by one or more semiconductor junction voltage drops.

29. An apparatus as claimed in claim 27 or 28 wherein one said reference signal is responsive to the level of the blanking level of said second clamped sync portion.

30. An apparatus as claimed in claim 27 or 28 wherein one said reference signal is responsive to the sync tip level of said second clamped sync portion.

31. An apparatus for deriving a logic level version of the sync portion of a video type signal, said sync portion having a number of levels N, one of which may be a blanking level, and where N may be two or more depending on the format of said video type signal, said apparatus including:

circuitry to provide a format signal changeable in response to the format of said video type signal;

circuitry responsive to said sync portion to generate at least a first separated sync signal;

circuitry for providing at least N–1 reference signal(s) in response to said sync portion and said first separated sync signal; and

circuitry responsive to said sync portion and said format signal and said reference signal(s) for comparing said sync portion to said reference signal(s) to provide said logic level version.

32. An apparatus as claimed in claim 31 wherein one said reference signal is responsive to the level of said sync portion which has the level closest to the peak white value of said video type signal.

33. An apparatus as claimed in claim 31 wherein said circuitry to provide a format signal is responsive to said video type signal to change said format signal in response thereto.

34. An apparatus as claimed in claim 31, 32 or 33 wherein N is two for NTSC or PAL type video signals and N is 3 for HDTV type video signals and where one said reference signal is provided for NTSC or PAL type video signals and at least two said reference signals are provided for HDTV type video signals, each which reference signals are responsive to at least one sync portion level.

35. A video sync pulse circuit responsive to composite sync pulses which may be part of a composite video signal said circuit operative to provide a reference voltage corresponding to the 50% level of sync, including in combination:

a) a coupling capacitor coupled to an input terminal to AC couple said composite sync pulses to a sync tip clamp circuit, said sync tip clamp circuit including a source of current operative to charge said coupling capacitor in a first direction and further including circuitry to charge said coupling capacitor in the opposite direction during at least a portion of the time said AC coupled sync tips surpass a reference, said charging action thus providing sync tip clamping to provide a sync tip clamped signal;

b) a buffer, responsive to said sync tip clamped signal to buffer same to provide a buffered signal;

c) a comparator responsive to said buffered signal and a reference to provide a compared sync signal;

d) a plurality of pulse circuits responsive to said compared sync signal from said comparator to provide a first sample and hold pulse in response to the leading edge of said compared sync signal and a second sample and hold pulse in response to the trailing edge of said compared sync signal;

e) a first sample and hold circuit responsive to said first sample and hold pulse and a DC restored form of said composite sync pulses to sample and hold the voltage level of sync tip;

f) a second sample and hold circuit responsive to said second sample and hold pulse and blanking level of said DC restored form of said composite sync pulses to sample and hold the voltage level of blanking;

g) a divider circuit responsive to the held voltage of sync tip and the held voltage of blanking to provide an in between voltage which is said reference voltage;

wherein circuitry used to accomplish one of elements a) through g) may be shared between two or more elements.

36. A video sync pulse separator circuit responsive to a composite video signal for providing horizontal and vertical sync pulses including in combination:

a) a coupling capacitor to AC couple said composite video signal to a sync tip clamp circuit, said sync tip clamp circuit including a source of current operative to charge said coupling capacitor in a first direction and further including circuitry to charge said coupling capacitor in the opposite direction during at least a portion of the time any AC coupled sync tip surpasses a reference, said charging action thus sync tip clamping to provide a sync tip clamped signal;

b) a buffer responsive to said sync tip clamped video signal to buffer said sync tip clamped video to provide a buffered signal;

c) a comparator responsive to said buffered signal and a reference to provide a compared sync signal;

d) a plurality of pulse circuits responsive to said compared sync signal from said comparator to provide a first sample and hold pulse in response to the leading edge of said compared sync signal and a second sample and hold pulse in response to the trailing edge of said compared sync signal;

e) a first sample and hold circuit responsive to said first sample and hold pulse and sync tip of a DC restored form of said composite video signal to sample and hold the voltage level of sync tip;

f) a second sample and hold circuit responsive to said second sample and hold pulse and blanking level of said DC restored form of said composite video signal to sample and hold the voltage level of blanking;

g) a divider circuit responsive to the held voltage of sync tip and the held voltage of blanking to provide an in between reference voltage;

h) a further comparator responsive to said reference voltage and comparison video to provide reference sync pulses, said comparison video being a version of said composite video signal of element a) having a known DC level;

i) a half horizontal pulse eliminator circuit responsive to said reference sync pulses to output horizontal rate pulses;

j) a vertical synchronizing filter circuit responsive to said reference sync pulses to output a vertical rate pulse;

k) a field synchronizing circuit responsive to at least circuit element j) and to the relationship of horizontal sync pulses and the leading edge of vertical sync to output a field synchronizing pulse signifying odd and even fields,

wherein circuitry used to accomplish one of elements a) through k) may be shared between a plurality of elements.

37. The video sync pulse circuit of claim **35** or **36** wherein element b) includes amplification, in element e) said first sample and hold pulse is delayed with respect to the leading edge of sync tip to allow said first sample and hold pulse to start within said sync tip and in element c) said buffered signal has reduced high frequency components as compared to said sync tip clamped signal of a).

38. The video sync pulse circuit of claim **35** or **36** wherein said comparator of element c) includes adjustment of the magnitude of the difference between said buffered signal and said reference value which adjustment is made in relation to the sync level of said buffered video to provide a reduction in comparator sensitivity to noise.

39. A method for processing a sync portion of a video type signal, said sync portion having a plurality of levels, comprising steps to:

a) a first separation of said sync portion to generate a first separated sync signal, including clamping the sync tip of said sync portion to a known level before said first separation;

b) generating a plurality of level signals each being representative of a level of a second clamping of said sync portion, at least one of said level signals is also generated in response to said first separated sync signal;

c) providing a reference signal in response to said plurality of level signals;

d) a second separation of said second clamped sync portion in response to said reference signal to provide a second separated sync signal which is a version of said sync portion.

40. A method for processing a sync portion of a video type signal, said sync portion having a plurality of levels, comprising steps to:

a) a first separation of said sync portion to generate a first separated sync signal, including clamping the sync tip of said sync portion to a known level established by one or more semiconductor junction voltage drops before said first separation;

b) generating a plurality of level signals each being representative of a level of a second clamping of said sync portion, at least one of said level signals is also generated in response to said first separated sync signal;

c) providing a reference signal in response to said plurality of level signals;

d) a second separation of said second clamped sync portion in response to said reference signal to provide a second separated sync signal which is a version of said sync portion.

41. A method as claimed in claim **39** or **40** wherein said step b) includes establishing one level of said sync portion at a known level in response to said first separated sync signal before said generating and with step d) performed on said second clamped sync portion having one level established of step b).

* * * * *

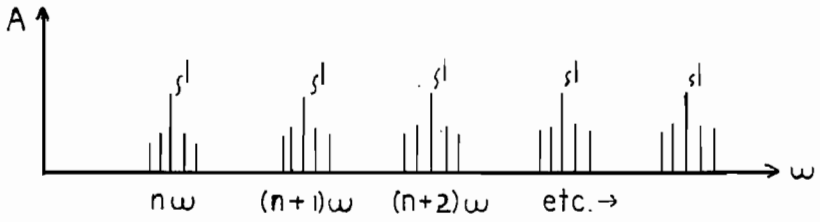


FIG. 1

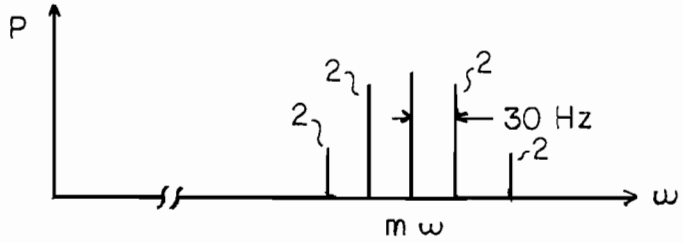


FIG. 2

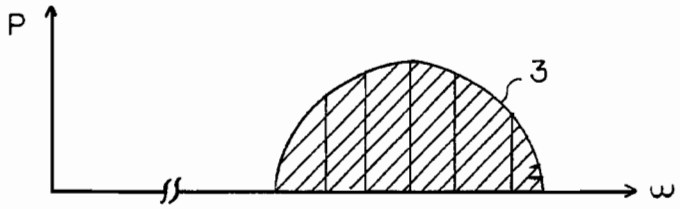


FIG. 3

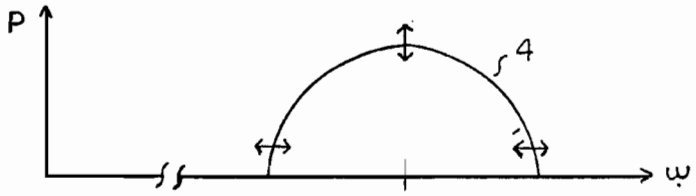


FIG. 4

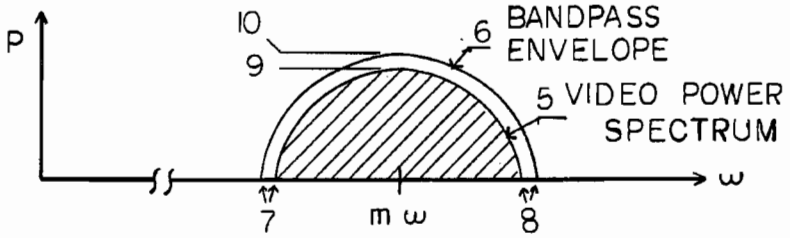


FIG. 5

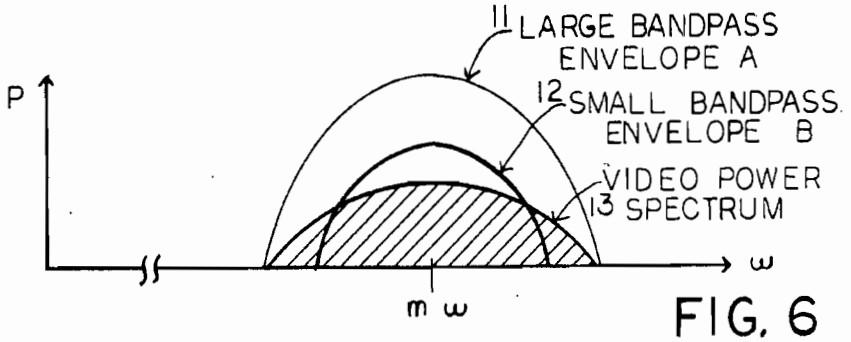


FIG. 6

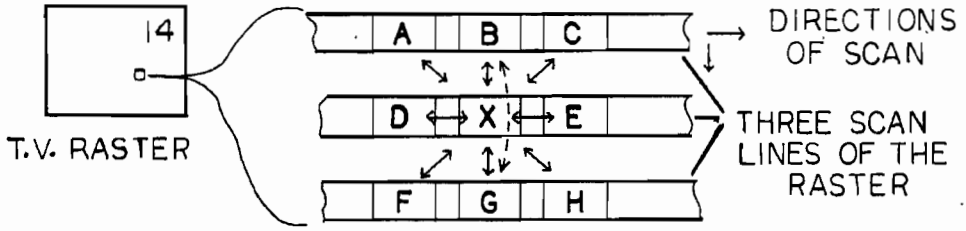


FIG. 7

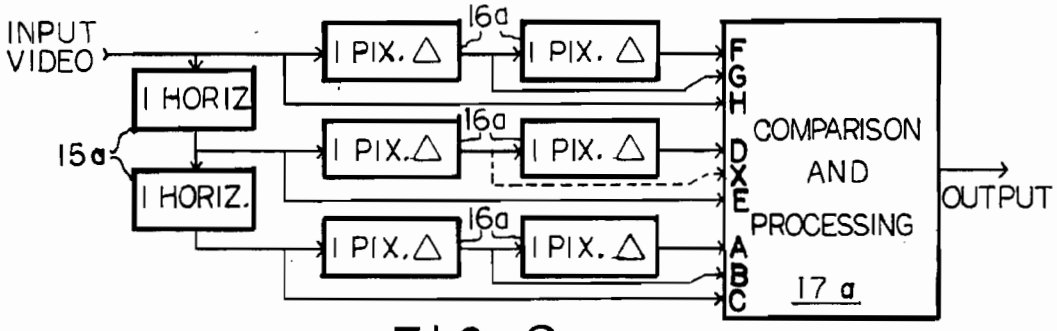


FIG. 8

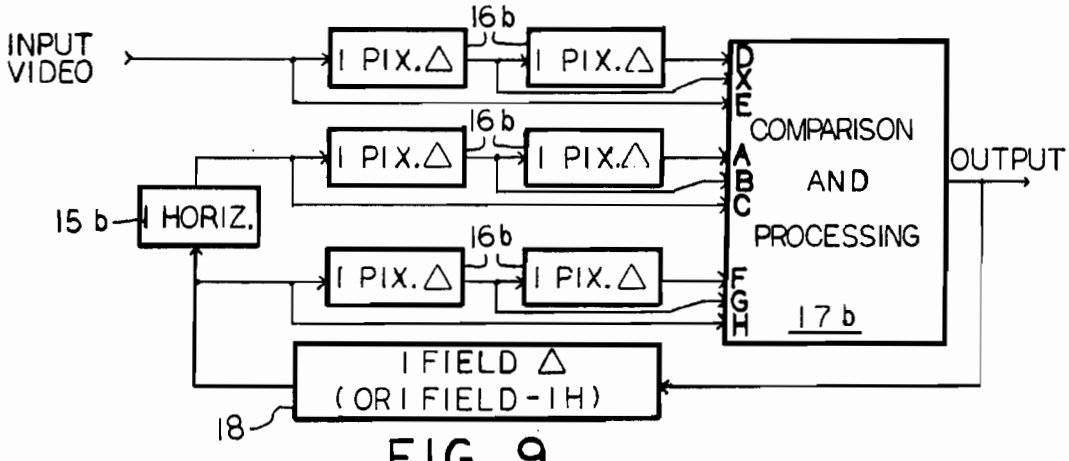


FIG. 9

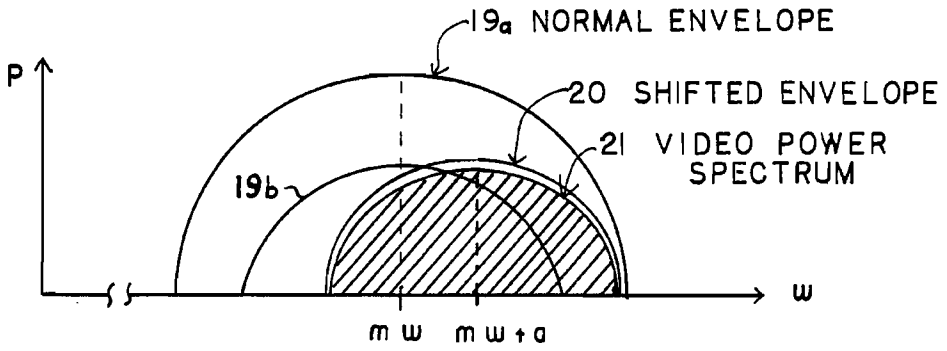


FIG. 10

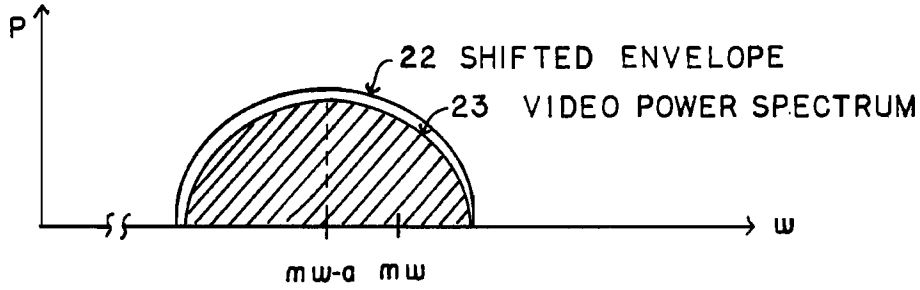


FIG. 11

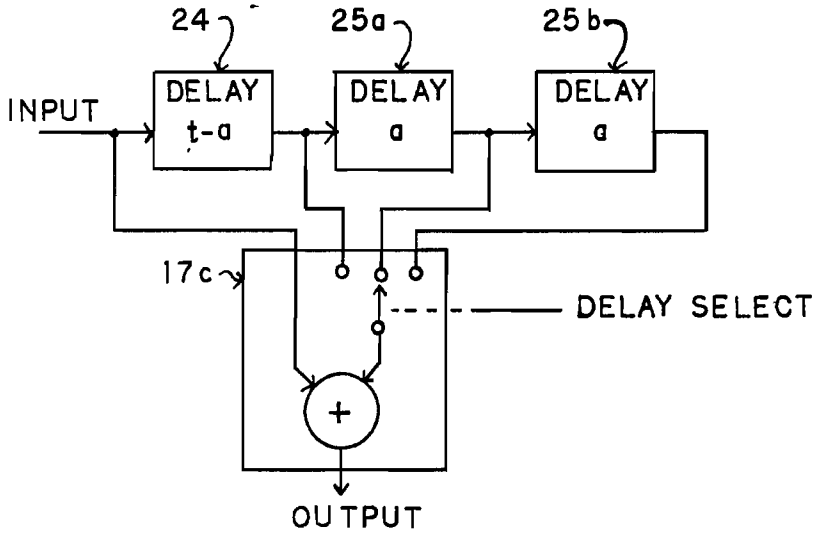


FIG. 12

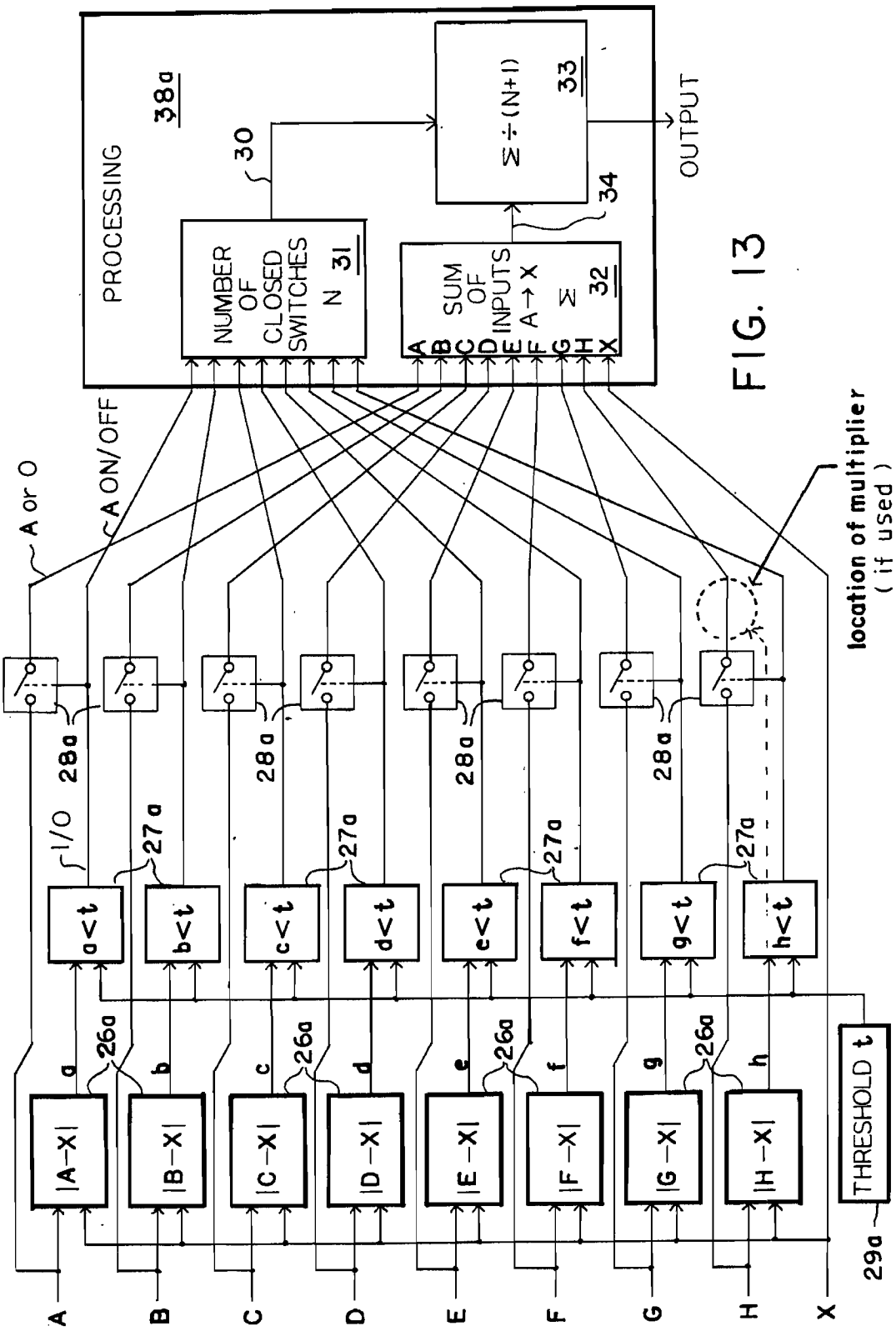

PROCESSING
38a
30
NUMBER OF CLOSED SWITCHES N 31
SUM OF INPUTS A→X Σ 32
A B C D E F G H X
Σ ÷ (N+1) 33
34
OUTPUT
A or 0
A ON/OFF
location of multiplier (if used)
I/O
28a
27a
a<t
b<t
c<t
d<t
e<t
f<t
g<t
h<t
26a
|A−X|
|B−X|
|C−X|
|D−X|
|E−X|
|F−X|
|G−X|
|H−X|
THRESHOLD t
29a
A
B
C
D
E
F
G
H
X

FIG. 13

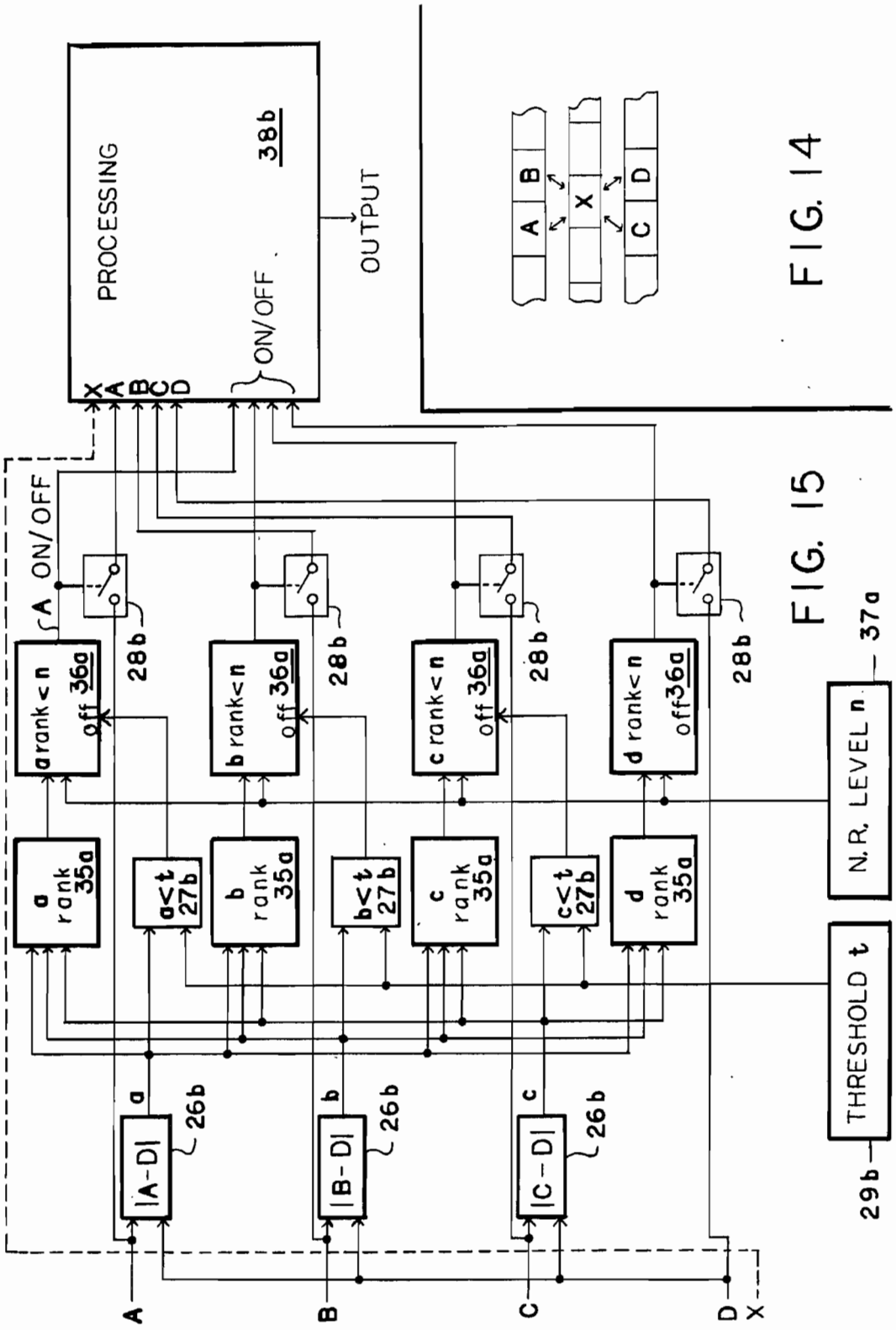


FIG. 14

FIG. 15

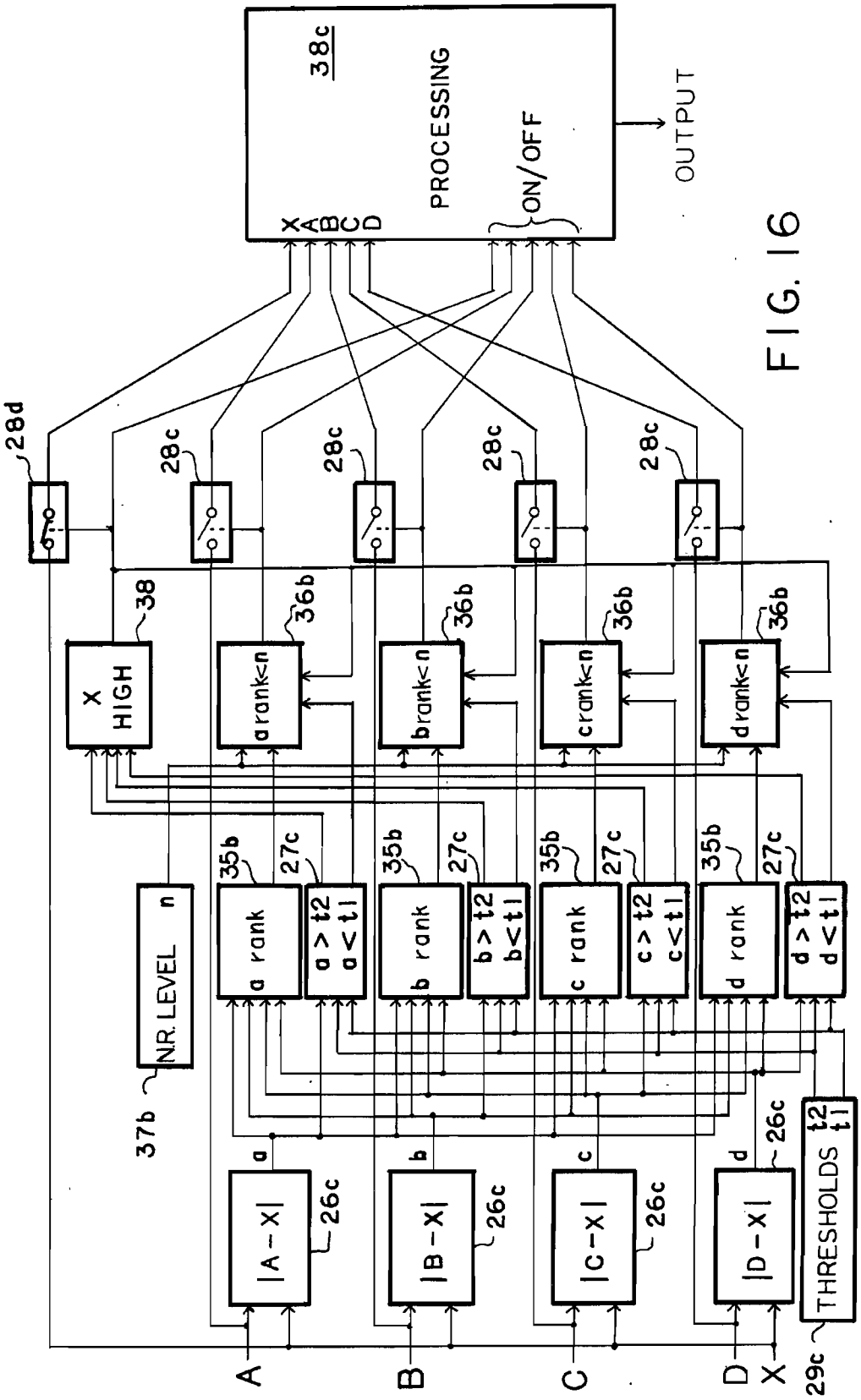

38c
PROCESSING
ON/OFF
OUTPUT
X A B C D
28d
28c
38
X HIGH
36b
a rank<n
b rank<n
c rank<n
d rank<n
35b
27c
a rank
a > t2
a < t1
b rank
b > t2
b < t1
c rank
c > t2
c < t1
d rank
d > t2
d < t1
N.R. LEVEL
n
37b
|A-X|
|B-X|
|C-X|
|D-X|
26c
THRESHOLDS
t2
t1
29c
A
B
C
D
X

FIG. 16

NOISE REDUCTION SYSTEM FOR VIDEO SIGNALS

This application is a continuation of Ser. No. 268,870, filed 06-01-81, now abandoned and a continuation-in-part of U.S. patent application Ser. No. 30,288 filed Apr. 16, 1979 now U.S. Pat. No. 4,305,091 entitled "Electronic Noise Reducing Apparatus and Method", which application in turn is a continuation-in-part of U.S. patent application, Ser. No. 763,904 filed Jan. 31, 1977, now abandoned, entitled "Electronic Noise Reducing Apparatus and Method."

Noise on video signals and in particular low amplitude random noise is a very troublesome problem in television systems. Several methods of removing this noise have been developed which include coreing, comb filters, and recursive temporal integration systems. Coreing systems are generally unacceptable because along with the noise a large amount of detail is lost. Line type comb filters have long been used for chroma separation, with a small signal to noise improvement, and now large scale digital noise reducers which utilize frame delays to implement recursive temporal integration or time averages, are available. Two such devices are described in detail in U.S. Pat. Nos. 4,058,836 Drewery et al. and 4,064,530 Kaiser et al. These recursive time integration systems do a fairly good job of noise reduction, but always introduce an artifact known as motion effect due to the infinite impulse response characteristic of recursive filters, and the problem of frame to frame video differences. The motion effect problem in general prevents the cascading of devices, and limits the amount of useful noise reduction of an individual unit.

It is the object of this invention to provide a high level of noise reduction similar to the temporal integration systems without the inherent motion effect artifacts, or loss of detail as in coreing systems. This is accomplished with a filter operating on picture elements in a continuous analog system, or a discrete sample time system such as would be provided in a digital or charge coupled device system, in either a recursive or non-recursive configuration. Because the filters delay times may be changed automatically in response to the motion of elements in the video, and because the number of coefficients of the filter may also be changed automatically, the bandpass characteristics of the filter may be automatically adjusted to fit the input video signal to a close degree.

Other objects and a fuller understanding of this invention may be had by referring to the following description and claims, taken in conjunction with the accompanying drawings, in which:

FIG. **1** is a typical video power spectrum with characteristic power clusters **1**;

FIG. **2** is a more detailed drawing of one of the power clusters with typical 30 hz. separated sidebands **2**;

FIG. **3** is a typical video power cluster envelope **3**;

FIG. **4** is a typical video power cluster envelope **4** which depicts characteristic envelope shape changes;

FIG. **5** is a typical video power cluster spectrum **5** having a peak amplitude **9**, with an upper band edge at **8** and a lower band edge at **7**, and a typical comb filter bandpass envelope **6** having a peak allowable amplitude **10** and having upper and lower band edges also at **8** and **7**;

FIG. **6** is a spread video power spectrum **13** with comb filter bandpass envelopes **11** and **12**;

FIG. **7** is a drawing of **3** scan lines from some random point in a television raster, showing the location of 9 picture elements A thru H and X;

FIG. **8** is a drawing of a typical delay configuration for the non-recursive form of the noise reducer, having 1 horizontal line delays **15***a*, 1 pixel delays **16***a* and comparison and processing circuit **17***a*;

FIG. **9** is a drawing of a typical delay configuration for the recursive form of the noise reducer having 1 horizontal line delay **15***b*, 1 pixel delays **16***b*, 1 field delay **18** and comparison and processing circuit **17***b*;

FIG. **10** is a shifted video power spectrum **21** with shifted bandpass envelope **20** and noise reducer bandpass envelopes **19***a* and **19***b*;

FIG. **11** is a shifted video power spectrum **23** with shifted bandpass envelope **22**;

FIG. **12** is an adaptable nonrecursive filter having delays **24**, **25***a*, **25***b* and processing circuit **17***c*;

FIG. **13** is a detailed block diagram of a comparison and processing circuit having inputs A thru H and X, absolute value difference computers **26***a*, magnitude comparators **27***a*, video switches **28***a*, threshold number **29***a*, processing circuit **38***a* composed of coefficient adder **31** with output **30**, pixel summer **32** with output **34** and divider **33**;

FIG. **14** is a drawing of 3 scan lines from a random point in a television raster showing the locations of pixels A thru D and X;

FIG. **15** is a detailed block diagram of a comparison and processing circuit having inputs A thru D and X with absolute value difference computers **26***b*, threshold number **29***b*, rank computers **35***a*, magnitude comparators **27***b*, rank magnitude comparators **36***a*, video switches **28***b*, processing circuit **38***b* and noise reduction level **37***a*;

FIG. **16** is a detailed block diagram of a comparison and processing block having absolute value difference computers **26***c*, rank computers **35***b*, dual magnitude comparators **27***c*, rank magnitude comparators **36***b*, video switches **28***c* and **28***d*, processing circuit **38***c*, X high computer **38**, noise reduction number **37***b* and threshold numbers **29***c*.

It is the object of video noise reduction systems developed as comb filters to provide a bandpass characteristic which matches the spectrum of the video signal to be improved thus rejecting the noise which is contained in the unused spectrum. The merit of these systems may be understood by inspecting the power versus frequency spectrum of video signals, which are shown in simplified graphic examples in FIGS. **1-4**. In FIG. **1** a typical power spectrum is shown with the characteristic power clusters **1** at harmonics of the horizontal scanning frequency w. FIG. **2** is a more detailed drawing of one of the harmonics mw, showing the sidebands **2** of each cluster which are spaced a nominal 30 hz apart in frequency for complex changing video. The 30 hz offset is a result of the frame repetition rate used and would be 25 hz for 50 cycle European systems. If one considers a single picture element, it is obvious that the lowest frequency component of the video signal corresponding to that element, if it is stationary, is the frame rate. In a static video signal, i.e., one scanning a non-changing scene, the amplitude and number of the 30 hz sidebands associated with a given harmonic power spectrum will vary according to the line to line changes in picture detail, and for this purely static signal any given side-

band group of a horizontal harmonic has no amplitude modulation or frequency modulation components with respect to time. In a normal video scene having motion and changing images, any of these 30 hz sidebands, 2 of FIG. 2, will have time changing amplitude and frequency components which will take up a part or all of the spectrum around the horizontal harmonic, this spectrum may be depicted as the envelope 3 shown in FIG. 3. The width and amplitude of the envelope will of course be independently changing with the scene information, as is shown by envelope 4 in FIG. 4. For the purpose of the following disclosure, reference to power and bandpass envelopes are in relation to one or more given horizontal harmonic power clusters within the video bandwidth.

In this high performance noise reduction device, the object is to model a comb filter such that the bandpass envelope of the teeth of the filter fit the expected video power clusters at the horizontal harmonics. A diagram of a video power envelope 5 and a comb filter bandpass envelope or tooth 6, for one of the 30 hz sideband groups is shown in a simplified graphic example in FIG. 5. In actual practice, the envelopes of FIGS. 3–6 would be much more complex if viewed on a spectrum analyzer or plotted with a high degree of accuracy, however these drawings will still serve to illustrate the important concepts relating to this invention. Obviously, the closer the bandpass envelope 6 fits the video power envelope 5 with respect to their upper and lower cutoff frequencies 8 and 7, the better the rejection of out of band noise and thus noise reduction of the signal will be. If the bandpass envelope also limits the video amplitude 9 to a level slightly higher than that needed to pass the video information as is shown by 10, thus high amplitude noise spikes will also be limited. Both envelopes 5 and 6 in FIG. 5 are representations of complex series of 30 hz elements. The devices in the previously mentioned Drewery and Kaiser patents operate to adjust the width of the bandpass envelope, i.e., changing the allowable number of the 30 hz elements within the bandpass envelope so that the entire video power envelope may be passed, while keeping the distance between upper and lower cutoff frequencies, or width of the bandpass envelope 6 as small as possible, however it is not possible to adjust the cutoff frequencies and width independently. In the device described by Kaiser et al. the coefficients of the input and delayed signals are changed in order to vary the noise reduction levels which causes the size of the bandpass envelope to change. It should be noted that by changing these coefficients that it is not possible to modify the shape of the bandpass envelope, i.e., to change the width independent of the amplitude, or to change the center frequency of the envelope of the 30 hz components. As shown in FIG. 6, when the video power spectrum 13 broadens due to changing video, the bandpass envelope may be increased as is shown in 11 to pass all of the video spectrum with very little noise reduction, or a compromise is set such as 12 which achieves moderate noise reduction and some loss of video information. As a result of the limited control over the shape, and position of the 30 hz components within the bandpass envelope, serious mismatching of the bandpass and power envelopes can occur, such as in FIG. 6.

The noise reduction system for electronic signals disclosed herein operates on a spatial technique in which each picture element within a television raster 14 is compared to the elements surrounding it such as X and A thru H respectively, as shown in solid line typically in FIG. 7, with said picture element being selectively combined with those surrounding elements which are similar to the central element in a product, a sum, a mean, a weighted average or similar mathematical process. The actual mathematical process used is relatively unimportant from a noise performance standpoint since all average and mean type processes give approximately the same level of noise reduction, however other image processes may be combined in this function as will be discussed later. It is important to note that for removing low amplitude noise the surrounding picture elements are not compared with each other, but only with the central element and there is no need to compute any two dimensional measure of the surface deviation or flexure about the central element. As was disclosed previously the surrounding elements do not have to be truly adjacent or symmetrically patterned, however experimental results indicate that the adjacent symmetrically patterned elements are best. Note, however, that surrounding elements can be directly compared as shown for example in dotted line in FIG. 7. The area covered by these the examined elements may be referred to as the inspection area. For the purpose of the following disclosure it will be assumed that these elements are discrete time elements such as samples in a digital system, however the disclosed concepts will apply equally to any continuous analog system where the elements are continuous and not broken or sampled into individual units. This may be effected in hardware by replacing all memories or shift registers used by digital systems with analog delay lines. Analog delay lines are of course available in either fixed delay length and variable delay length configurations.

The above process may take on either a recursive or nonrecursive form and may operate on a varying number of surrounding elements depending on the desired cost versus performance and complexities involved. The sampling system used and as a result the alignment of the sampled elements from line to line will also affect the number of elements used and delay structure to arrive at those elements. One should note that the elements shown in FIG. 7 are aligned vertically and those of FIG. 14 are offset from line to line showing 2 common systems which may be used. The particular considerations of sampling schemes will be obvious to one skilled in the art and will not be discussed further. A typical nonrecursive system would look like that of FIG. 8 and a recursive system like that of FIG. 9. The dotted line FIG. 8 recognizes that the element x can be omitted from the comparison and processing of the signals. FIGS. 13, 15 and 16 disclose various embodiments of the comparison and processing circuitry of FIGS. 8 and 9. The object and operation of the comparison and processing circuits are the same for any system; only the configuration of the delays 15, 16 and 18 used to generate the central and surrounding picture elements X and A through H respectively is changed in order to optimize the system for a particular application. The changes from non-recursive to recursive systems are essentially the same as for textbook digital filters and will not be extensively discussed. Inputs to the comparison and processing circuit 17*a* in FIG. 8 and 17*b* of FIG. 9 are labeled A thru F and X corresponding to where these elements appear in the raster as shown in FIG. 7.

As was previously mentioned, the video 30 hz sideband shape is a result of both the line to line detail

changes and frame to frame detail changes. A special case where a displayed image changes in its raster position from frame to frame while the image itself remains relative unchanged frequently occurs in video. An example of this would be where a camera pans a fixed scene with little detail around the edges of the frame. The effect of this type of changing video is to greatly broaden and frequency shift the 30 hz components of the video power envelope while the amplitude remains relatively constant such as shown in FIGS. **10** and **11**. If one considers a given pixel which is moving in the frame, that element's lowest frequency component is no longer the frame rate that it was when stationary, but has been changed by the amount of motion. If the element were to move 2 scan lines up per frame, the lowest frequency component would be 1 frame less 2 H, thus giving a positive frequency shift by an amount a to the video power spectrum such as is shown by **21** in FIG. **10**. This situation gives rise to the mismatching of envelopes similar to that previously mentioned, and is shown by **19***b* and **21** of FIG. **10**. If the picture elements were to move down in the frame a negative frequency shift such as shown by **23** of FIG. **11** would be created. Because the envelope center frequency cannot be shifted the two options available to a temporal integration noise reducer such as those previously discussed are to increase the bandpass envelope like **19***a* of FIG. **10** to broaden the allowable number of 30 hz components to pass all of the components of the video information but provide little noise reduction, or to set a compromise position such as shown by **19***b* of FIG. **10** which provides moderate noise reduction, and some loss of video information. Unfortunately, in most state of the art noise reducers, the smaller envelope **19***b* will be used and most of the video information which is lost contains frame to frame detail information. In a recursive type of system this lost detail is accentuated due to the infinite impulse response characteristic, giving a smear effect on the edges of moving images which is known in the industry as motion effect. The primary reason for motion effect is the lack of ability of noise reducers to change the shape and frequency position of the bandpass envelope, independent of the allowable amplitude characteristic to match the video envelope adequately. The mechanism needed to accomplish this is an adaptive time delay system which can track moving picture elements from frame to frame or field to field.

A simple diagram of such an adaptive system is shown in FIG. **12**. If the 3 position switch of **17***c* is in the middle position the filter will have bandpass teeth at some frequency spacing w which is determined by the length of delays **24** and **25***a*. If one assumes **24** is a delay of t−a, and **25***a* and *b* each have a delay of a with t being much larger than a, then the 3 position switch will be able to select delays of t−a, t and t+a. The switch selection will then have the effect of shifting the bandpass envelope in frequency by a small amount determined by a. The bandpass envelope will look like **20** and **22** of FIGS. **10** and **11** and one can see that by selecting the proper switch position the filter's frequency characteristic can be made to closely match the video power spectrum. The operation of the filter may be simply explained by assuming that the delay t is equal to the repetition period, i.e., 1/frequency of a sine wave signal to be passed by the filter. The middle switch position will be selected and the input signal will be summed with the input signal which has been delayed by t or one wave length thus giving an output equal to twice the input. If another signal is input which has a wave length of 2t there will be no output since the input will be combined with the signal delayed by t, which corresponds to a 180° phase shift, i.e., two signals of exact opposite phase are added with a sum of 0. If the wanted signal now shifts either up or down in frequency by an amount 1/a a different switch position may be selected to adjust the filter bandpass characteristic accordingly. Thus for a signal having a repetition period of t+2a the right switch position would need to be selected to give the optimum delay, and for a signal having a repetition period of t the left switch would be selected. In general for this type of filter the delay should be selected to match the repetition period of the wanted signal. The method of determining what delay length is to be used is a nontrivial matter, and is one of the inventive concepts of this device and method, as will be discussed later in this disclosure. One skilled in the art can envision a system where the three delays and switch would be replaced with a single variable length delay such as a CCD device clocked with a variable frequency clock.

Referring to FIG. **13**, the least complex comparison and processing system, each of the pixels from the delays is input to an arithmatic block **26***a* along with pixel X, where the absolute value of the difference between X and the respective pixel is computed. Each of these absolute value differences, a for pixel A, b for B, etc. is compared to a threshold t, **29***a*, in blocks **27***a* to determine if the difference is less than the threshold **29***a*. If the difference is less than the threshold, a switch **28***a* is closed which allows the corresponding pixel to be input to the processing circuit **38***a*, otherwise the switch **28***a* is opened which inputs a zero, this action allows only picture elements which are similar to X to be input to the processing circuit **38***a*. For the purpose of this explanation the threshold is assumed to be a fixed number, however one skilled in the art recognize that it would be useful to make the threshold automatically variable in response to the signal to noise ratio of the incoming video signal, or to the video content of said signal. The threshold would be adjusted to a relatively small value for good S/N ratios, and a large value for poor S/N ratios. In section **32** the processing circuit sums all of the pixels including pixel X, which are input to it. Section **31** adds the coefficients of the elements input to the processing circuit at section **32**, either by summing all the coefficients of the switches (one or zero) or alternately by adding multiplier coefficients as discussed later, and section **33** divides **34**, the sum of the picture elements by the total of coefficients of picture elements summed **30**, thus computing the average of those elements. Alternately the root mean square, product or other combination could be used to generate a replacement value or output for element x. This average is the normalized noise reduced signal which is output from the device. Of course each of the switch functions **28***a* could be replaced with or supplemented by a multiplier (or divider) as shown in the H signal path in FIG. **13**, to perform a weighted average such as a gaussian weighted response of the elements selected. Such a system might perform the weighting function in a fixed on/off mode or the weighting might be adjusted according to the computed difference A thru H of FIG. **13**, or alternately according to the rank which will be discussed later. For example the weighting given to element A might be (1−a') where the function is defined by A(1−a') where A is the value of element A, a'

is the normalized value of a, i.e., a÷(2× maximum allowable value of A). The multiplier could also be used in order to provide weighting of each element to perform other image operations such as unsharp masking, lag reduction and spatial enhancement, or as a replacement for the switch **28***a*. The coefficient of the multiplier (or divider) would be controlled by the difference computed in **26***a* or the threshold comparison output from **27***a*. Typical noise reduction results output from the processing means would then be like (A+B+C+-D+E+F+G+H+X)÷9 where all differences are less than t, or (A+B+C+X)÷4 where only differences a, b and c are less than t or only X where all differences are greater than t. For spatial enhancement one typical output would be (jA+kB+jC+kD-+kE+jF+kG+jH+X)÷m where the coefficients j and k are fixed multiplier constants, or zero as determined by **26***a* and **27***a*, and m is the normalization number, i.e., the sum of the absolute value of the coefficients +1, corresponding to **30**. The actual weighting function and values used would depend on the quality of the video signal being processed. If the signal were soft due to the use of a low quality camera for origination, spatial enhancements would be used to sharpen the video images to a more pleasing level, if the video contained lag due to low light conditions a lag reduction operation could be performed. Actual coefficients to accomplish these functions have been developed by computer image processing devices which operate on still pictures, and a study of computer image processing will reveal actual coefficients which can be used to correct video image defects. A typical set of values for a high pass (detail enhancement) filter would be j=−0.25 and k=−0.5. If A, B, and C had differences less than t the output would then be [(−0.25A)+(−0.5B)+(−0.25C)+X]÷2.

In FIG. **15** a more complex processing and comparison system for a five element scheme such as is shown in FIG. **14**, is illustrated. FIG. **15** contains the same difference computing arithmetic block, **26***b*, corresponding to **26***a* for each element, the same threshold comparison system, **29***b* and **27***b* corresponding to **29***a* and **27***a* respectively, the same picture element switches, **28***b*, corresponding to **28***a* and the same processing circuit **38***b* corresponding to **38***a* to average the selected pixels as does the system of FIG. **13**. FIG. **15** does differ by the addition of a rank computers **35***a* and rank to noise reduction level comparison **36***a* for each difference. It is the function of the rank computers **35***a* to compare each difference a thru d to all of the other differences to determine how many of the other differences it is greater than. Each difference is given a rank from 0 to N where N is one less than the total number of differences, in this instance N=3. For example, if the differences had magnitudes of: a=3, b=4, c=9, d=5, the ranks would be a=0, since a is larger than none of the other differences, b=1, c=3, d=2. It is of course possible for two or more differences to have the same rank, if they had the same difference value. Each difference's rank is in turn compared to the noise reduction level **37***a* in **36***a*, if the rank is smaller than the N.R. level **37***a* and if the difference is smaller than the threshold t, **29***b*, the corresponding switch **28***b* for that element is closed inputting said element to the processing circuit **38***b*. Switch **28***b* could be replaced or augmented by a multiplier or other operation as in the previous example. As with the threshold **29***a* of the previous example, the N.R. level **37***a* could be adjustable in response to input video. Since any difference greater than **29***b* will probably have a high rank it also would be possible to delete **29***b* and **27***b* at a sacrifice in performance, and small cost savings. The processing circuit will compute the average of all elements input to it as in the system **38***a* of FIG. **13**. If either the difference for an element is larger than the threshold t, **29***b*, or the rank of that difference is larger than the N.R. level, **37***a*, then the switch **28***b* or multiplier for that element is forced to input a zero to the processing circuit **38***b*. Of course individual thresholds or N.R. levels could be used for each element, which would give preference to the direction of elements averaged and the switch **28***b* could be replaced with or augmented by a multiplier as discussed previously.

If one assumes that in the area of inspection the picture had moved 1 vertical line up in the past field of time, then element X which is currently input to the device would be from the same point on the televised image as that which is output from the memory corresponding to the area immediately below X, on the line from the preceding field. This point is represented by the junction between pixels C and D of FIG. **14** (or pixel G of FIG. **7**). These elements would then have a very low rank, since they correspond to approximately the same point on the image as x, and would be input to the processing block. The filter will have tracked the movement causing the time delay to be adjusted accordingly, by the process of rank selection of pixels. One can see that it would be wise to use enough elements in this system to cover all of the possible locations that an input pixel could move to or from within a one field (or alternatively 1 frame) amount of time, in order for the filter to track any possible motion in the input video signal. Referring to FIG. **16**. It will be seen that the system of FIG. **16** is similar to that of FIG. **15**, except that 2 thresholds are output from **29***c*, 2 comparisons are made in each of the magnitude comparators **27***c*, an extra circuit, the X high circuit **38** has been added which controls a video switch **28***d* in the X video line input to the processing circuit **38***c*. In the previously discussed circuits of FIG. **13** and FIG. **15** it has been assumed that pixel X would always be averaged with the other elements input to the processing circuit.

In some video applications, in particular digital applications, a noise situation exists which corresponds to a digital bit error which will cause a gross amplitude change in an individual pixel. An example of this would be in an application using a solid state RAM or in a digital data transmission channel where a MSB bit is defective due to noise. In the circuits of FIGS. **13** and **15** this gross amplitude change occurring on pixel X would cause all of the magnitude comparators to sense differences greater than the threshold t, thus effectively passing pixel X to the output unaveraged. In the circuit of FIG. **16** the magnitude comparators essentially compare the differences to two thresholds, t1 and t2. Threshold t1 can be assumed to have the same value and effect as does t of FIGS. **13** and **15**. Threshold t2 is a much higher threshold used to detect gross amplitude differences. The t2 threshold comparison for each difference is input to the X high circuit **38**. If a number of differences, nominally two or more, have exceeded the t2 threshold, **38** opens the video switch **28***d* for pixel X and forces the other rank comparators to close their respective video switches thus inputting all pixels except X into the processing circuit **38***c*. In the simplest configuration, processing circuit **38***c* will average all the

pixels input to it, thus outputting this value for the noise reduced value of X.

Experimental results have shown the above processing system adequate for occasional random gross amplitude errors, however when these gross amplitude errors increase in frequency it may be desirable to average only a small number of surrounding pixels, those which are closest in magnitude to each other. These close magnitude pixels represent the minimum brightness gradient or the surface contour having the least amount of deflection or change within the area under inspection, and their average statistically represents the highest probability of the true noise free value of X. For the pixels within the area of FIG. 7 the minimum gradient would be the smallest magnitude of A-H, B-G, C-F or D-E which would be determined with difference circuits like *26b* operating on each pair of elements and rank computer *35a* of FIG. **15**, i.e., the minimum gradient would also have the smallest rank. The output of the processing system would be the average of those two pixels having the smallest difference if X was determined to have a gross error. The circuitry which would need to be added to the processing circuit of FIG. **16** to accomplish a minimum gradient average is minimal and would be an elementary design task to one skilled in the art. Similar minimum brightness gradient circuitry was also discussed by Graham in U.S. Pat. No. 3,009,016. It should be noted however that if pixel X does not suffer from gross amplitude noise, and has a difference less than threshold t, the system of either FIG. **15** or **16** will inherently compute an average of pixels because of the operation of the rank computers and rank threshold comparison, as was previously discussed.

In many systems which operate on digital video signals there is circuitry included to detect bit or gross errors as part of such systems. In these systems it would be unnecessary to include the X high circuitry **38** and the associated threshold t2 and comparison circuitry since errors on pixel X have already been detected. The external system error detector would merely need to be coupled to the rank computers *36b*, the X video switch *28d* and processing means *38c* as was the X high circuit **38**.

The element x need not be used in the treatment of normal television signals (element x containing very little information not present in neighboring pixels) or in defective television images (wherein the neighboring pixels statistically have a high probability of representing the true noise free value of x). The neighboring pixels could thus be directly compared with the results used to replace a different pixel. A mathematical process to do this could be accomplished by deleting element x from the processing means in FIGS. **15** and **16**, using a different subtrahend in FIG. **13**, or otherwise.

The operation of the noise reduction device has been discussed in relation to FIGS. **13**, **15** and **16** in order to clearly explain how the device functions, however it will be clear to one skilled in the art that several of the functions could be combined or implemented in a different fashion as is convenient in order to optimize the design to meet a particular set of goals such as low cost, portability or high performance. It is considered obvious that the hardware used to implement any of the various functions such as the delays *15a, b* and **18** could be shared with another device, such as would be the case if this invention were constructed as a secondary feature or option of another device such as a television frame synchronizer, or that the video signal could be output from the main memory via a different port thus giving the video output a variable delay and essentially the ability to perform a timebase corrector or synchronizer capability.

Of particular interest for state of the art television systems is the recursive system shown in FIG. **9** because of its unique and efficient relationship when used in a 2:1 interlace system. In the arrangement of FIG. **9** the input video picture element X is compared to those surrounding it (see FIG. **7**). However it may be noted that by carefully selecting the length of the large delay **18**, so that it provides at its output the line above the input line, (which may require a change in delay length to compensate for interlace on even or odd fields) elements ABCFG and H will be from the field previous to element X. This situation has the requirement of approximately a 1 field delay for **18**, rather than a 1 frame delay which is most often used in recursive temporal average systems, with the obvious cost advantage. By combining the system configuration of FIG. **9** with the processing and comparison system of FIG. **15** or FIG. **16**, which has been expanded to handle **9** total elements, a very good cost vs. performance ratio is achieved. One can see that by the previously described system of FIG. **15** or FIG. **16** of selecting pixels which surround X to average together in this recursive scheme of FIG. **9**, a form of adaptive recursive comb filter is effected. It is most important to note that the delay used is variable by the amounts controlled by the selection of the surrounding elements. For example, in FIG. **9**, if pixel C is selected the delay is 1 H more than if pixel H is selected. Referring to the previous discussion Line relating to the shape of the bandpass envelope one should understand that it is this variable delay arrangement which coupled with averaging variable numbers of pixels, which may have variable weighting, can cause both the width and allowable amplitude of, as well as the position of 30 hz components of the bandpass envelope to change independently and automatically in order to provide a close fit to the video power spectrum envelope, as well as providing spatial image processing.

The above described system which utilizes a field delay proves in practice to be extremely cost effective and of high performance when compared to frame recursive devices which are currently commercially available. To one skilled in the art it should be obvious that there are many variations of this system which may be constructed to fit a given need. In particular a much more elegant system could be built which utilizes a full frame delay thus allowing an input pixel to be compared with those pixels surrounding it in both the previous field and the previous frame. Less or more than the suggested nine elements could also be used with a group of central elements being compared to a group of surrounding elements. A system could also be built which allows the comparison of one or more input pixels to a number of the pixels surrounding it, but from the previous frame or a multiple number of frames or fields. It may be noted that in all cases the delayed element corresponding to input element X i.e. that element corresponding to the same point on the raster as X need not be used if a sufficient number of surrounding elements are used, since it is reasonable to assume that the delayed element corresponding to X contains very little information not already contained in those pixels which surround it, for normal television scenes.

What is claimed is:

1. Apparatus for reducing noise on an input televison video signal which apparatus contains a comparison circuit means responsive to said input video signal to compare a central picture element of said video signal to at least one of the surrounding picture elements of said video signal to determine the difference thereof and to further compare said difference to a threshold, said threshold adjusted automatically in response to said input television video signal, and a processing circuit responsive to said picture elements and said comparison to sum portions of said surrounding element and said central element if said difference corresponding to said surrounding element is less than said threshold, with said portion of surrounding element being decreased otherwise, which decreased portion may be zero and which sum is the noise reduced value substituted for said central element by said processing circuit before said signal is output from said apparatus.

2. Apparatus for reducing noise on an input televison video signal which apparatus contains a comparison circuit means responsive to said input video signal to compare a central picture element of said video signal to at least one of the surrounding picture elements of said video signal to determine the difference thereof and to further compare said difference to a threshold, a processing circuit responsive to said picture elements and said comparison to sum portions of said surrounding element and said central element if said difference corresponding to said surrounding element is less than said threshold, with said portion of said surrounding element being decreased otherwise, which decreased portion may be zero and which sum is the noise reduced value substituted for said central element by said processing circuit before said signal is output from said apparatus, a second comparison circuit responsive to differences from multiple surrounding elements wherein said differences are compared to each other allowing said multiple surrounding elements to be ranked according to their respective differences with only a number of said surrounding elements which have the smallest differences being summed with said central element which number of surrounding elements may be a number set by an operator or may be responsive to said input video signal in either delayed or undelayed form.

3. Apparatus as claimed in claim 2 wherein the number of said surrounding elements combined is responsive to the amount of noise on said input video signal in delayed or undelayed form.

4. Apparatus as claimed in claim 2 wherein the number of said surrounding elements combined is responsive to the information content of said input television video signal in delayed or undelayed form.

5. A method for reducing noise on a video signal which noise may result from errors occurring in a video signal system with said method containing a comparison step to compare a central video element of said video signal to two or more of the video elements surrounding said central element as viewed on the television raster to determine the difference thereof, and a processing step responsive to said comparison to determine if said difference is greater than a threshold and to replace a noisy central video element with a combination of at least two surrounding elements which may be the same or different elements as said compared elements with said replacement ocuring when said central video element differs from said two or more of the compared surrounding elements by more than said threshold.

6. A method as claimed in claim 5 wherein said two combined surrounding samples have a difference which is less than the difference of any two other surrounding samples as determined by a further comparison step.

7. A method as claimed in claim 5 wherein said two combined surrounding samples are adjacent to said noisy central video sample and constitute the minimum brightness gradient across said noisy video sample as determined by said further comparison step.

8. The method of claim 5 wherein the surrounding video elements of the combination are from the scan line above and scan line below the central video element and from the same field.

9. A method for reducing noise on a set of pixels derived from an optical image including the steps of comparing two pixels to determine the difference thereof, comparing said difference to a reference to determine the larger thereof and replacing a given pixel with a combination of other pixels in response to said comparison to said reference, said combination representing a noise reduced given pixel.

10. The method for reducing noise of claim 9 wherein the two pixels being compared to determine the difference thereof are different than the given pixel replaced.

11. The method for reducing noise of claim 10 wherein the given pixel is used in the combination of pixels.

12. The method of claim 9 wherein the given pixel is located between two compared pixels.

13. The method of claim 9 wherein the given pixel and compared pixels are each on a separate scan line from the same field and are aligned in a straight line on the raster.

14. The method of claim 9 wherein the given pixel and compared pixels are from the same point on the raster but each located in a different frame.

15. A method for reducing noise on a video signal comprising the steps of comparing a given pixel to other pixels to determine whether the difference between each of such other pixels and the given pixel is less than a reference threshold level, combining said given pixel and those other pixels that are within said reference threshold level of said given pixel, the total number of pixel signals used in this combining varying and outputing the combination, this combination increasing the apparent signal to noise ratio of the video signal.

16. Method as claimed in claim 15 wherein said combinations includes summing said given pixel and those other pixels within said reference threshold of said given pixel and dividing said sum by the total number of pixels summed.

17. A method for reducing noise on an electronic signal derived by scanning a image comprising the steps of comparing a given element of said signal to each of two or more other elements of said signal to determine the difference thereof, comparing each difference to the other differences to determine which of said other elements has the smallest corresponding difference and combining the element having the smallest corresponding difference with at least said given element to provide a noise reduced element which may be substituted for said given element.

18. A method for reducing noise on a signal derived by scanning an image comprising the steps of establishing a reference threshold level, comparing a central pixel to adjacent pixels to determine whether the absolute value of the difference between each of such adjacent pixels and the central pixel is less than said refer-

ence threshold level, and computing an average of said central pixel and those adjacent pixels that are within said reference threshold level of said central pixel, the total number of pixel signals used in computing this average varying and outputing this average as the value of said central pixel, this averaging increasing the apparent signal to noise ratio of the video signal.

19. A method for reducing noise on a signal derived by scanning an image comprising the steps of establishing a reference threshold level, comparing the level of a central pixel to the levels of a plurality of the surrounding pixels to determine whether the absolute value of the difference between each of such surrounding pixels and the central pixel is less than said reference threshold level, computing the sum of the levels of said surrounding pixels that are within said threshold reference level of said level of said central pixel plus the level of said central pixel, computing the number of pixels summed, dividing said sum by said number to determine an average value for the levels of similar pixels, and outputing said value for said central pixel, this process increasing the apparent signal to noise ratio of the video signal.

20. A method for reducing noise on a video signal comprising the steps of establishing a reference threshold level, comparing the level of a first pixel to the levels of a plurality of the adjacent pixels to determine whether the absolute value of the difference between each of the compared adjacent pixels and said first pixel is less than said reference threshold level, computing the sum of the levels of said compared adjacent pixels that are within said threshold reference level of said level of said first pixel plus the level of said first pixel, computing the number of pixels summed, dividing said sum by said number to determine a value for the levels of similar pixels, and outputing said value for said first pixel, this process reducing the apparent noise of the video signal.

21. A method for reducing noise on a video signal comprising the steps of comparing the level of a given pixel to the level of neighboring pixels to determine whether the difference between each of said neighboring pixels and said given pixel is less than a reference threshold level, computing the sum of the levels of said neighboring pixels that are within said threshold reference level of said level of said given pixel plus the level of said given pixel, computing the number of pixels summed, dividing said sum by said number to determine a value for the levels of similar pixels, and outputing said value for said given pixel, this process increasing the apparent signal to said noise ratio of the video signal.

22. An apparatus for reducing noise on a series of pixels derived from a video signal, said apparatus comprising means to compare a given pixel to other pixels to determine whether or not the difference between each of such other pixels and the given pixel is less than a reference threshold level, and means to compute an average of said given pixel with those other pixels that are within said reference threshold level of said given pixel, the total number of pixel signals used in computing this average varying and means to output the average as the value of said given pixel, this averaging increasing the apparent signal to noise ratio of the video signal.

23. An apparatus for reducing noise on a series of pixels derived from a video signal comprising means of establishing a reference threshold level, means of comparing a central pixel to surrounding pixels to determine whether the difference between each of such surrounding pixels and the central pixel is less than said reference threshold level, means to average said central pixel and those surrounding pixels that are within said reference threshold level of said central pixel, the total number of pixel signals used in this average varying and means to output this average as the value of said central pixel, this averaging increasing the apparent signal to noise ratio of the video signal.

24. Apparatus for reducing noise on a group of pixels derived from a video signal including in combination means responsive to the difference between a given pixel and at least one other pixel to compare said difference to two threshold levels to determine the greater of said difference and each of said threshold levels and means for substituting a combination of two or more pixels for said given pixel in response to said comparisons.

25. A method for reducing noise on a set of pixels derived from an optical image including the steps of comparing two neighboring pixels to determine the difference thereof, comparing said difference to a reference to determine the larger thereof and replacing a third neighboring pixel located between said first two neighboring pixels with a combination including neighboring pixels in response to said comparison to said reference, said combination representing a noise reduced third pixel.

26. Method of claim **25** where first two pixels are chosen so that they have the same color subcarrier phase.

27. The method for reducing noise of claim **25** wherein the two neighboring pixels are combined to produce the combination of the neighboring pixels used to replace the third pixel.

28. The method for reducing noise of claim **27** wherein the third neighboring pixel is also used in the combination of the neighboring pixels.

29. The method for reducing noise of claim **25** wherein the reference is a percentage of signal type reference.

30. The method of claim **25** wherein said set of pixels consists of three pixels taken from three consecutive scan lines from the same field of an NTSC video signal with said third neighboring pixel being from the central scan line of said three scan lines and with one said compared neighboring pixel being from one of the other of the three scan lines and the other said compared neighboring pixel being from the third scan line.

31. The method of claim **25** wherein said combination of pixels is made such that noise is reduced on the color subcarrier.

32. The method of claim **25** wherein determining said difference includes subtracting a first pixel from a second pixel, and further including taking the absolute value of the result.

33. The method of claim **25** wherein said pixels include the color subcarrier of an NTSC video signal.

34. The method of claim **25** wherein said pixels are represented in digital form.

35. The method of claim **25** wherein said pixels are represented in analog form.

36. A method for reducing noise on a video signal comprising the steps of selecting neighboring picture elements from the signal, examining said elements to determine their respective levels, ranking said elements according to their respective levels, combining all said elements within a chosen rank to produce a replacement

value and outputing said replacement value in the place of one of said elements within chosen rank, this processing increasing the apparent signal to noise ratio of the video signal.

37. A method for reducing noise on a video signal comprising the steps of selecting a first and neighboring picture elements from the signal, examining said first and neighboring elements to determine their respective levels, setting a threshold, examining the levels of said neighboring elements to determine whether the level of any of said neighboring elements are within the level of said threshold of the level of said first element, ranking said neighboring elements within said threshold of said first element, combining all said within threshold neighboring elements within a chosen rank and outputing said combination of all said within threshold neighboring elements within said chosen rank in the place of said first element, this process increasing the apparent signal to noise ratio of the video signal.

38. A method for reducing noise on a video signal comprising the steps of selecting neighboring picture elements from the signal, selecting a reference, examining the levels of said elements to determine whether the level of any of said elements are within said reference of the other of said elements, combining said elements that are within said reference to each other, to produce a replacement value and outputing said replacement value of said elements that are within said reference of each other in place of one of said element that is within said reference of each other, this increasing the apparent signal to noise ratio of the video signal.

39. A method for reducing noise on a video signal comprising the steps of selecting a first and neighboring picture elements from the signal, examining said elements to determine their respective levels, setting a threshold, comparing the levels of said neighboring elements to determine whether the level of any of said neighboring elements are within said threshold of said first element, combining said neighboring elements that are within said threshold of said first element, and outputing said combination of said neighboring elements that are within said threshold of said first element in place of said first element, this process increasing the apparent signal to noise ratio of the video signal.

40. A method for reducing noise on a video signal comprising the steps of selecting neighboring picture elements from the signal, selecting a reference, comparing the levels of said elements to determine whether any of said elements are dissimilar by more than said reference from the others of said elements, combining some of said elements that are within said reference of each other, to produce a replacement value and outputing said replacement value of some of said elements that are within said reference of each other in place of one of said elements that is dissimilar by more than said reference of the others of said elements, this process increasing the apparent signal to noise ratio of the video signal.

41. A method for reducing noise on a video signal comprising the steps of selecting a first and neighboring elements from the signal, setting a threshold, comparing the levels of said neighboring elements to the level of said first element to determine whether the level of all of said neighboring elements are dissimilar by more than said threshold from said first element, and if all of said neighboring elements are dissimilar by more than said threshold from said first element then combining said neighboring elements and outputing said combination of said neighboring elements in place of said first element, this process increasing the apparent signal to noise ratio of the video signal.

42. The method of preserving detail in a noise reduced video signal wherein noise reduction is performed by combining a group of three or more pixels and substituting said combination for one pixel of said group, including the step of comparing two or more pixels of said group to determine the difference thereof, comparing said difference to a reference to determine the larger thereof, and inhibiting said substitution when said difference exceeds said reference.

43. The method of preserving detail in a noise reduced video signal which is the chroma subcarrier portion of an NTSC television video signal wherein noise reduction is performed by combining a first element and two neighboring elements of the input NTSC television video signal, said combination being the noise reduced value substituted for said first element, including the step of comparing two of said elements which are normally combined to determine if they are similar within a threshold value of each other, the step allowing said substitution to be made if said compared elements are similar within said threshold and inhibiting said substitution if said compared elements are not similar within said threshold thereby outputing said first element uncombined.

* * * * *

United States Patent [19]

Cooper

[11] **Patent Number: 4,573,070**

[45] **Date of Patent: Feb. 25, 1986**

[54] **NOISE REDUCTION SYSTEM FOR VIDEO SIGNALS**

[76] Inventor: **J. Carl Cooper**, 1373 Sydney Dr., Sunnyvale, Calif. 94087

[21] Appl. No.: **615,666**

[22] Filed: **May 31, 1984**

Related U.S. Application Data

[63] Continuation of Ser. No. 268,870, Jun. 1, 1981, abandoned, which is a continuation-in-part of Ser. No. 30,288, Apr. 16, 1979, Pat. No. 4,305,091, which is a continuation-in-part of Ser. No. 763,904, Jan. 31, 1977, abandoned.

[51] **Int. Cl.**[4] **H04N 9/64**

[52] **U.S. Cl.** **358/36**; 358/167; 358/37; 358/166

[58] **Field of Search** 358/167, 166, 162, 36, 358/37, 163, 170, 160, 213; 364/515; 382/50, 51, 54

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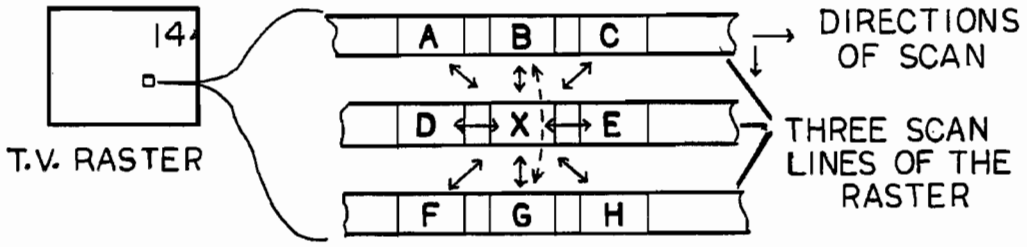
Primary Examiner—Michael A. Masinick

Attorney, Agent, or Firm—Woodling, Krost, Rust & Hochberg

[57] **ABSTRACT**

Noise reduction on a video signal is achieved by an adaptive filter system which is capable of automatic changes in filter parameters. This inventive concept includes an automatic method of independently changing both the width and center frequency of the teeth of a comb type bandpass envelope of the filter, as well as adjusting the amplitude response of the filter, independent of the bandpass characteristics, in order to closely match the filter bandpass response to the power spectrum of the video signal being processed, thus rejecting noise in those portions of the spectrum not being used by the video signal. The filter system herein disclosed also provides an adaptive spatial processing of the video signal thus further improving said signal by enhancing detail in the image and by smoothing low amplitude noise in relatively detail free areas of the picture.

43 Claims, 16 Drawing Figures



US005459524A

United States Patent [19]

Cooper

[11] Patent Number: 5,459,524

[45] Date of Patent: Oct. 17, 1995

[54] **PHASE MODULATION DEMODULATOR APPARATUS AND METHOD**

[76] Inventor: **J. Carl Cooper**, 15288 Via Pinto, Monte Sereno, Calif. 95030

[21] Appl. No.: **351,722**

[22] Filed: **Nov. 18, 1994**

Related U.S. Application Data

[63] Continuation of Ser. No. 792,725, Nov. 18, 1991, abandoned.

[51] **Int. Cl.**[6] **H04N 9/45**; H04N 9/455

[52] **U.S. Cl.** **348/507**; 348/508; 348/498; 348/539; 348/639

[58] **Field of Search** 348/497–498, 348/505–509, 536, 537, 539, 549, 638, 639, 641; 358/320, 323, 324, 325, 326; H04N 9/45, 9/455

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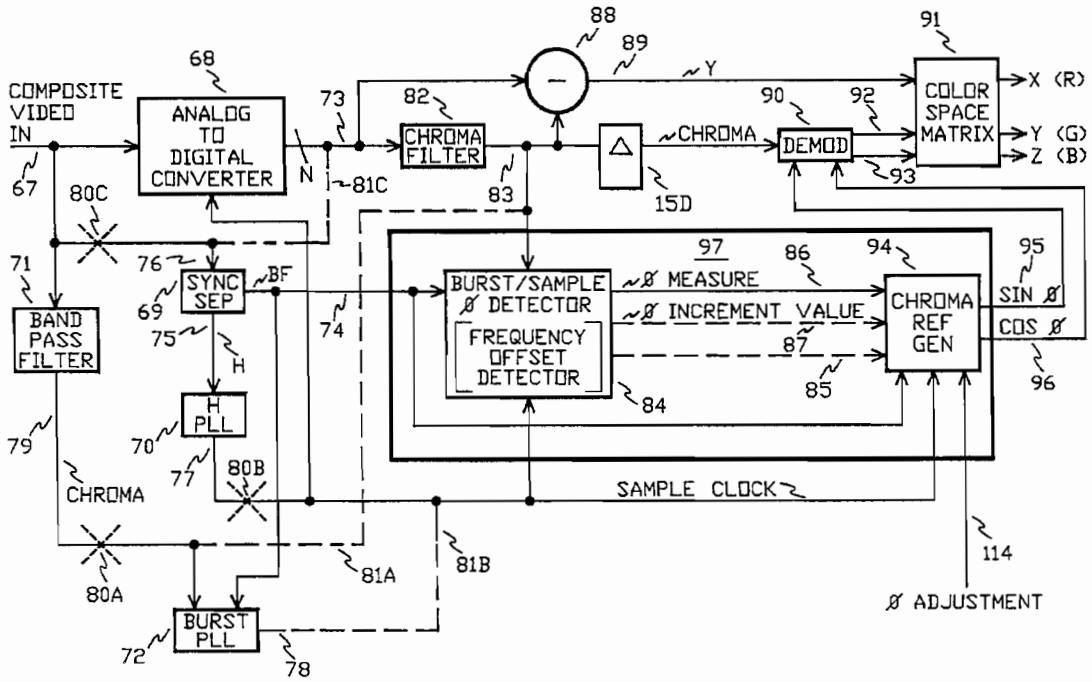
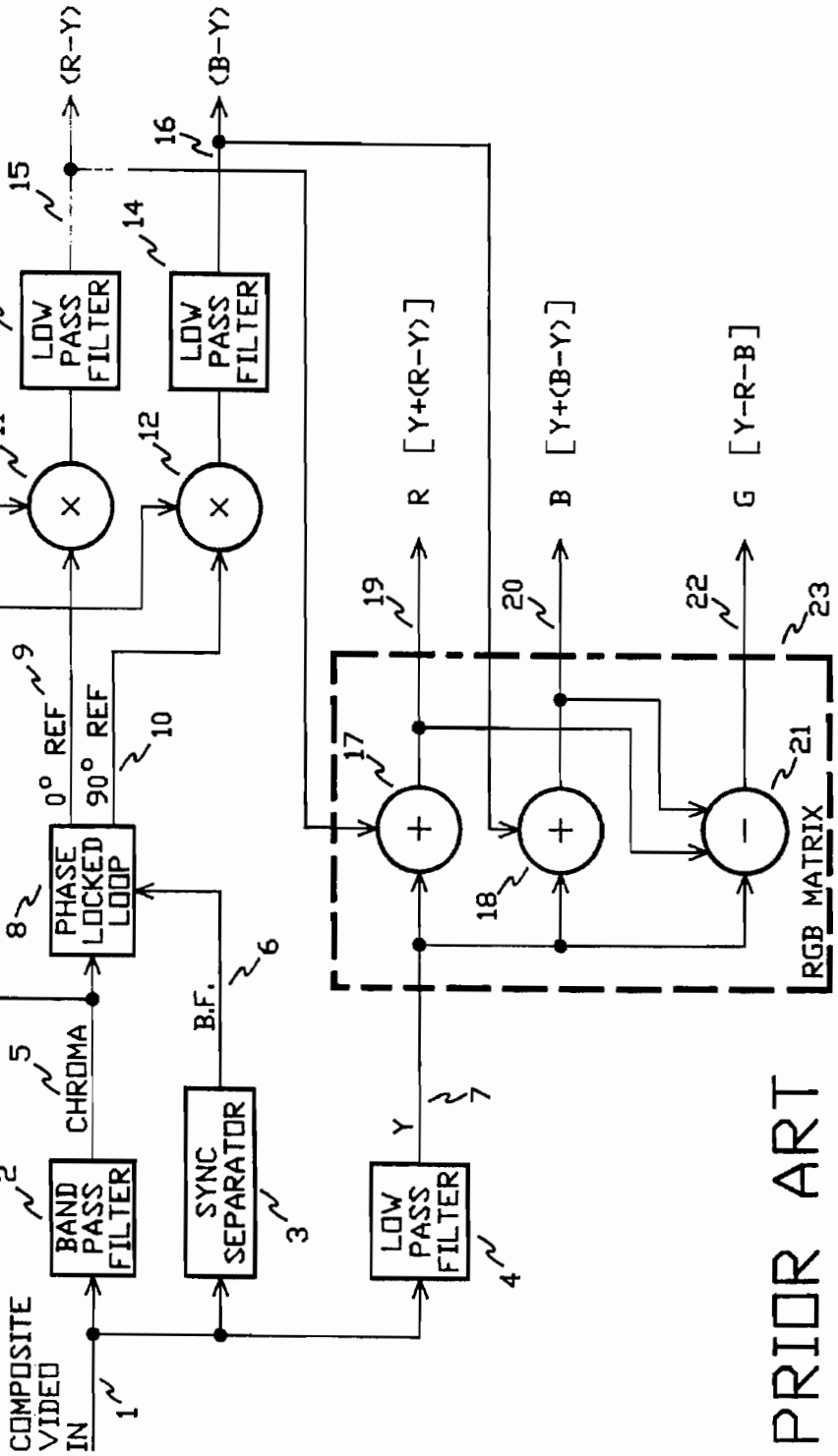
Primary Examiner—James J. Groody
Assistant Examiner—Michael H. Lee

[57] **ABSTRACT**

This invention is for a reference generator and demodulator for recovering information which has been phase, modulated on (or encoded on) a carrier. The inventive concepts described herein include a novel reference measurement circuit including a sampler and phase measurement circuit to measure the carrier reference's phase and/or frequency relative to a discrete time sampling phase and frequency, and a demodulator reference signal generator to generate properly phased reference signals for use by the phase demodulator circuit. The invention is particularly useful for decoding chroma difference signals of PAL and NTSC television video signals. It is suited to be implemented in digital form, operating on digitized signals thereby deriving all of the benefits normally expected of digital signal processing, including precision, freedom from drift and freedom from alignment. The invention is also particularly well suited to implementation by integrated circuit.

47 Claims, 7 Drawing Sheets

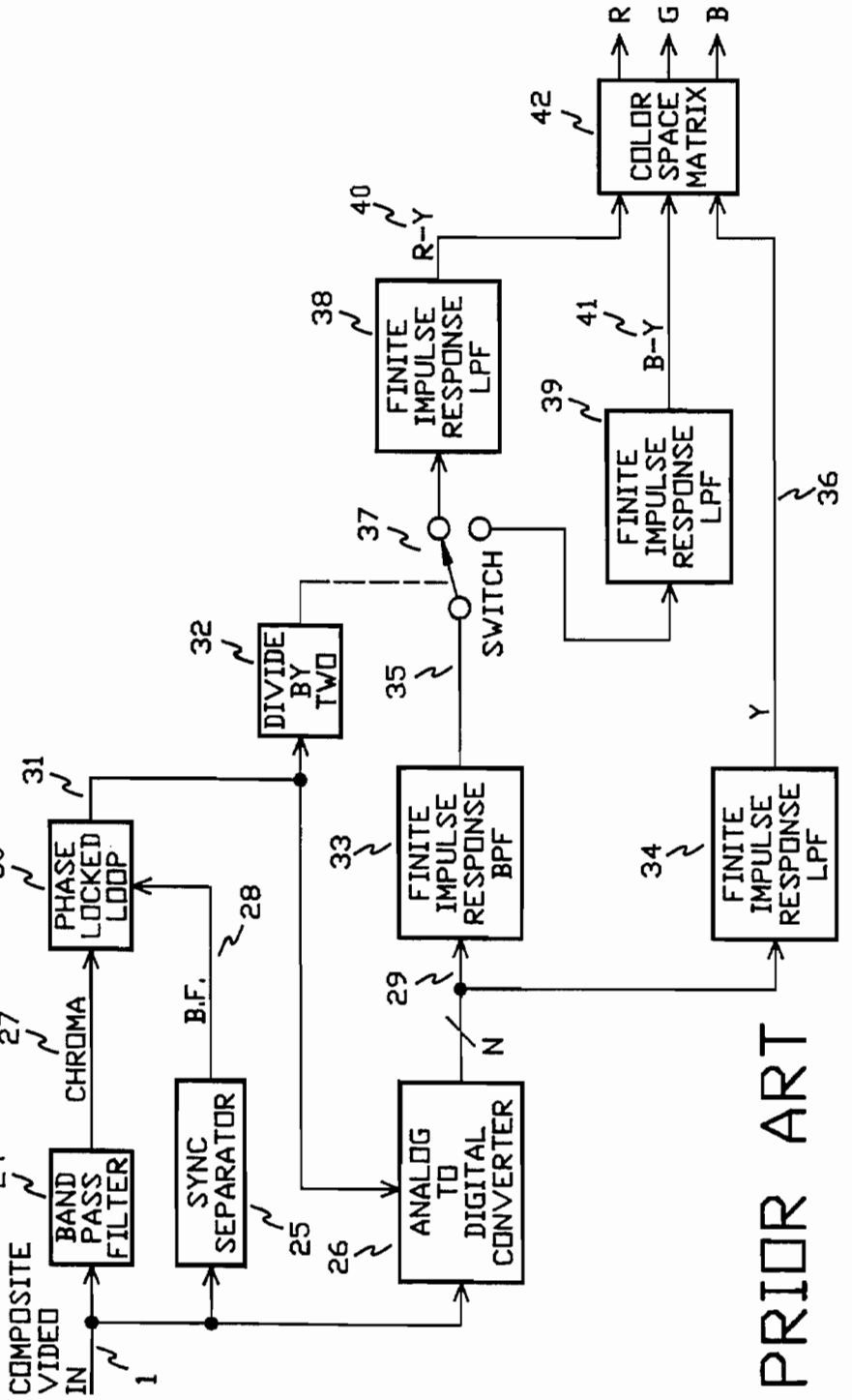




PRIOR ART

ANALOG R-Y, B-Y CHROMA DECODER

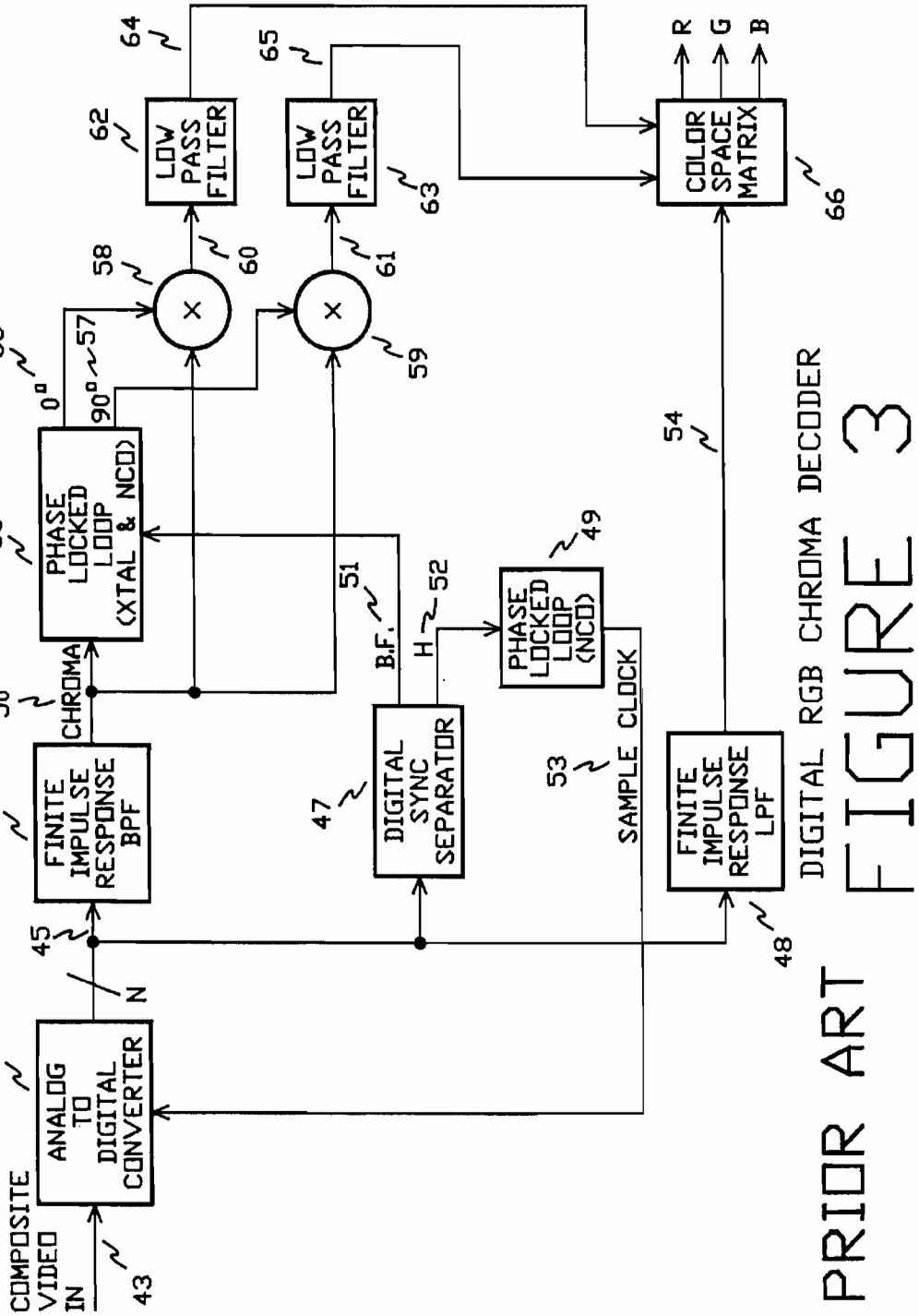
FIGURE 1



PRIOR ART

DIGITAL RGB CHROMA DECODER

FIGURE 2



PRIOR ART FIGURE 3

DIGITAL RGB CHROMA DECODER

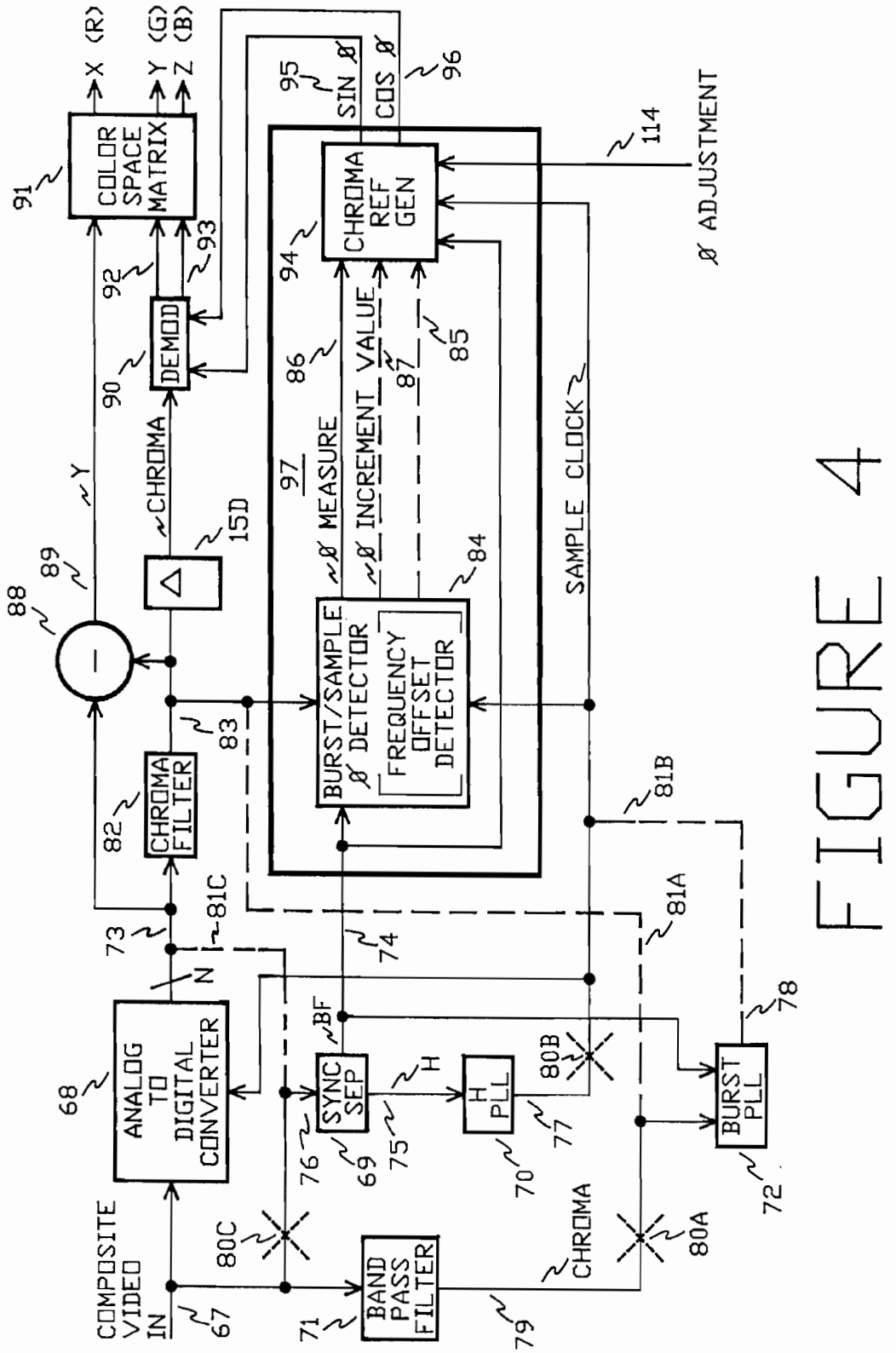

COMPOSITE VIDEO IN
67
ANALOG TO DIGITAL CONVERTER
68
BAND PASS FILTER
71
SYNC SEP
69
H PLL
70
BURST PLL
72
CHROMA FILTER
82
CHROMA
DEMOD
90
92
93
COLOR SPACE MATRIX
91
X (R)
Y (G)
Z (B)
CHROMA REF GEN
94
SIN Ø
COS Ø
95
96
Ø ADJUSTMENT
114
BURST/SAMPLE Ø DETECTOR
FREQUENCY OFFSET DETECTOR
84
Ø MEASURE
97
Ø INCREMENT VALUE
87
85
86
SAMPLE CLOCK
Y
89
88
15D
83
73
74
81A
81B
81C
78
77
75
76
80A
80B
80C
79
BF
H
N
CHROMA

FIGURE 4

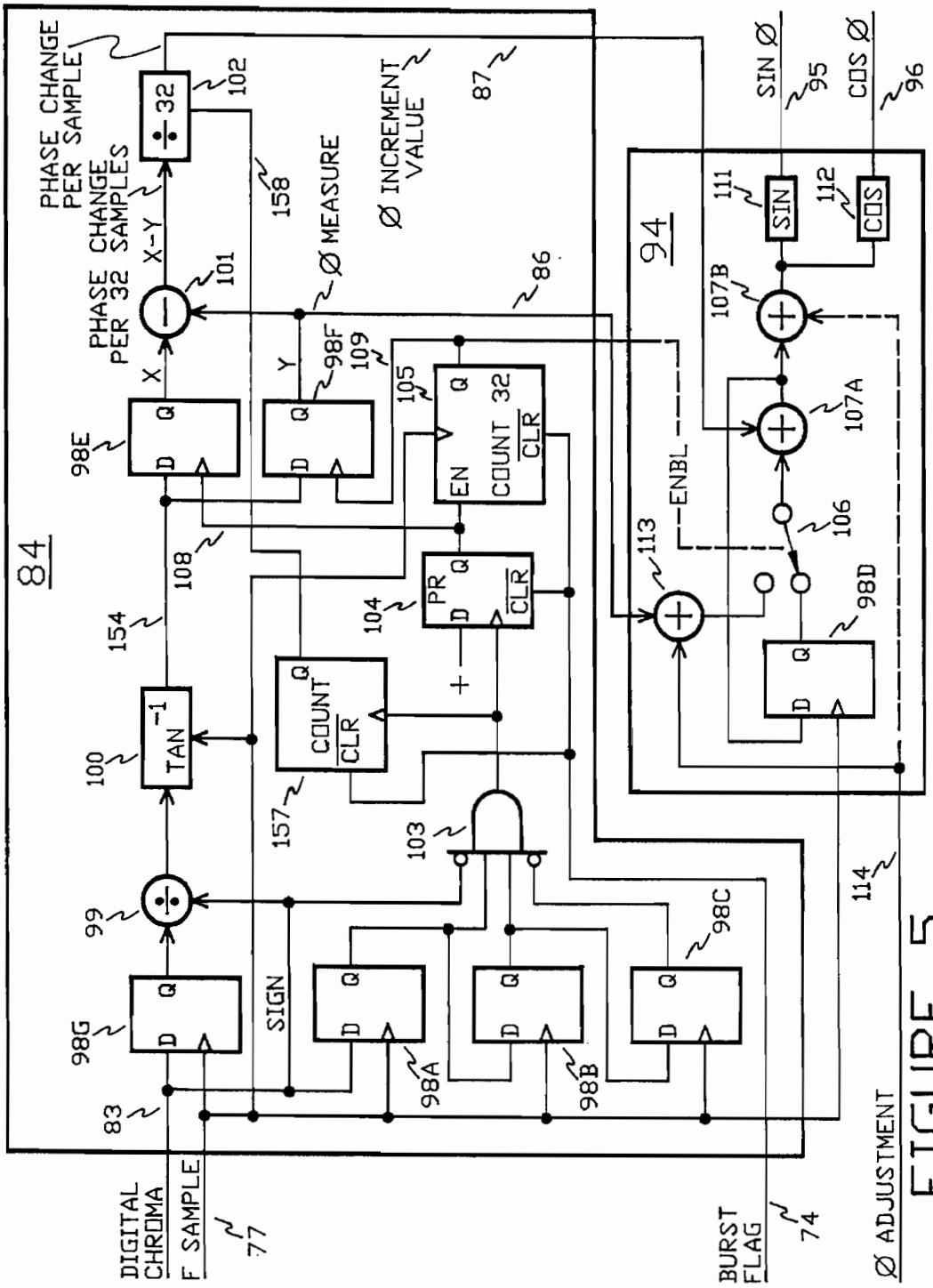

84
94
PHASE CHANGE PER SAMPLE
PHASE CHANGE PER 32 SAMPLES
X-Y
÷ 32
102
101
158
Ø MEASURE
Ø INCREMENT VALUE
87
86
SIN Ø
COS Ø
95
96
111
112
SIN
COS
107B
107A
106
ENBL
113
98D
98E
98F
109
105
COUNT 32
CLR
EN
PR
104
108
154
100
TAN -1
COUNT
157
103
99
98G
SIGN
98A
98B
98C
83
114
DIGITAL CHROMA
F SAMPLE
77
BURST FLAG
74
Ø ADJUSTMENT

FIGURE 5

$$\text{VALUE A} = \text{SIN}\ \alpha \cdot \text{AMPLITUDE}$$

$$\therefore \frac{A}{\text{AMPLITUDE}} = \text{SIN}\ \alpha$$

$$\text{VALUE B} = \text{SIN}\ (90^\circ - \alpha) \cdot \text{AMPLITUDE} = \cos\alpha \cdot \text{AMPLITUDE}$$

$$\therefore \frac{B}{\text{AMPLITUDE}} = \cos\alpha$$

$$\frac{\text{SIN}\ \alpha}{\cos\alpha} = \frac{\frac{A}{AMP}}{\frac{B}{AMP}} = \text{TAN}\ \alpha$$

$$\therefore \text{TAN}\ \alpha = \frac{A}{B}$$

$$\text{TAN}\ \alpha = \text{LOG}^{-1}\ (\text{LOG A} - \text{LOG B})$$

FIGURE 6

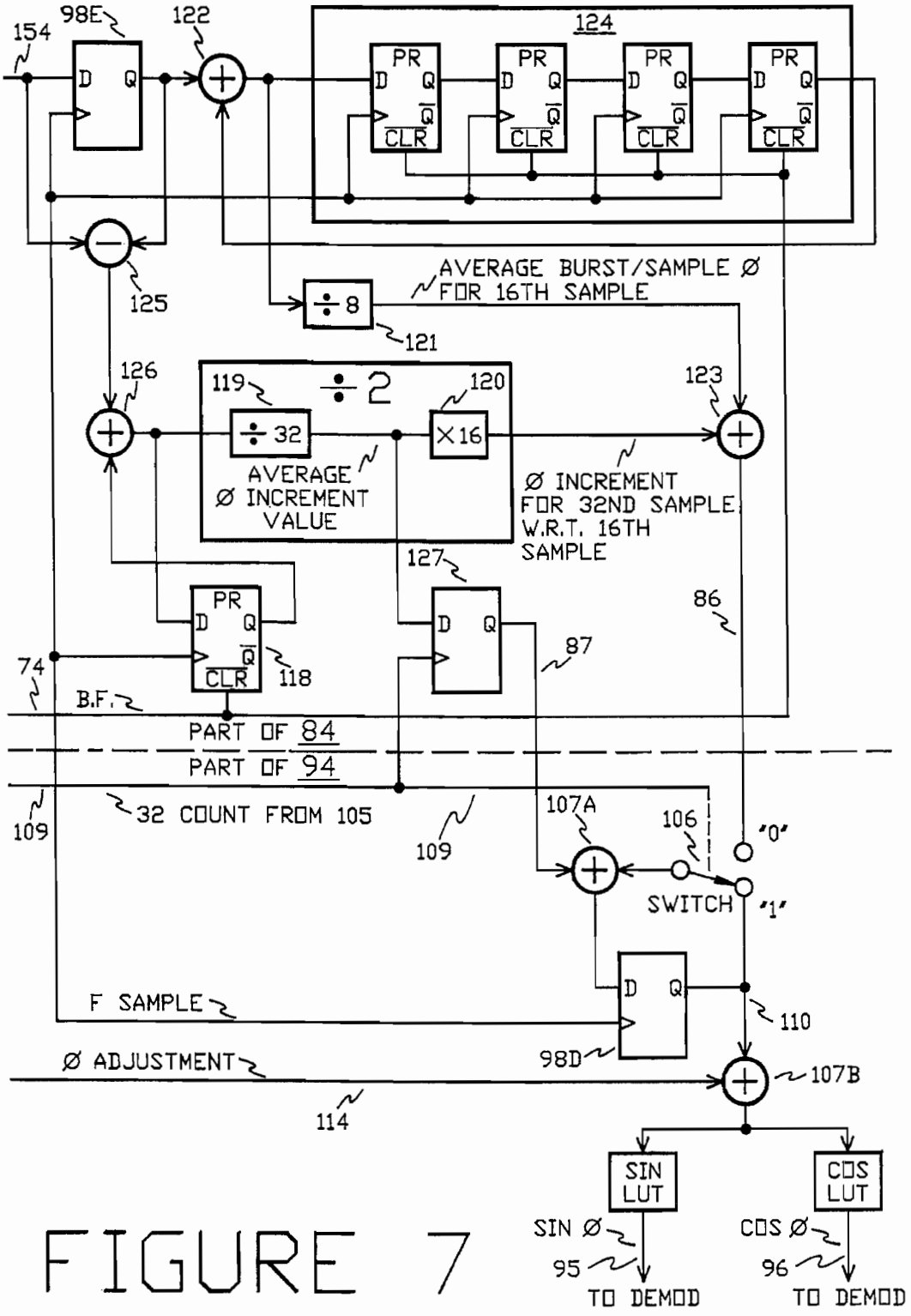

154
98E
122
124
PR
D Q
CLR
125
÷ 8
AVERAGE BURST/SAMPLE Ø FOR 16TH SAMPLE
121
126
119
÷ 2
120
123
÷ 32
×16
AVERAGE Ø INCREMENT VALUE
Ø INCREMENT FOR 32ND SAMPLE W.R.T. 16TH SAMPLE
127
86
87
74
B.F.
118
PART OF 84
PART OF 94
109
32 COUNT FROM 105
107A
106
"0"
"1"
SWITCH
F SAMPLE
110
98D
Ø ADJUSTMENT
114
107B
SIN LUT
COS LUT
SIN Ø
COS Ø
95
96
TO DEMOD

FIGURE 7

PHASE MODULATION DEMODULATOR APPARATUS AND METHOD

This application is a continuation of application Ser. No. 07/792,725, filed Nov. 18, 1991, now abandoned.

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates to the field of phase and amplitude modulating and demodulating carriers and subcarriers, and in particular to the modulating and demodulating of PAL and NTSC video chroma signals and the like which are carried on a quadrature (as well as other angle) phase and amplitude modulated subcarrier in the video signal.

2. Description of the Prior Art

The prior art contains many circuits for performing modulating and demodulating in phase modulation systems. A typical chroma demodulator is shown in FIG. **1** which shows a composite video input **1** from which composite video is coupled to Band Pass Filter (BPF) **2** which passes the chroma subcarrier of the video **5**, sync separator **3** which provides a burst flag signal (BF) **6** in response to the video sync, and low pass filter (LPF) **4** which passes the luminance (Y) portion **7** of the video signal. A phase locked loop (PLL) **8** receives the chroma **5** and burst flag **6** and phase locks an oscillator to the reference chroma burst of signal **5**, providing continuous chroma reference signals in quadrature **9** and **10**. The quadrature reference signals **9** and **10** are multiplied with the chroma signal in multipliers **11** and **12**, respectively, to effect the phase demodulation of the subcarrier. The resultant signals are low pass filtered (LPF) by **13** and **14** to remove the subcarrier and harmonic signals from the demodulated signals which in this example are Red-Luminance (R-Y) **15** and Blue-Luminance (B-Y) **16**.

Other demodulation angles have been used, such as I and Q, however in this prior art example, R-Y and B-Y is assumed. The R-Y and B-Y signals are then passed, along with the Y signal, to the color matrix **23** where the RED (R) **19**, GREEN (G) **20** and BLUE (B) **22** signals are derived by combining elements **17**, **18** and **21**, respectively. This type of prior art chroma demodulator is widely used and works fairly well, however due to its analog nature it requires alignment and precision components to achieve any moderate degree of performance. In addition, the PLL must be a crystal type, if it is to be relatively low in cost, or must be a very complex sync and burst locked circuit such as described in U.S. Pat. No. 4,026,041. The circuit does not lend itself to implementation in digital form, mainly due to the complexities of implementing a suitable VCO and PLL **8** to generate the quadrature reference signals **9** and **10**.

FIG. **2** shows another prior art demodulator embodiment having BPF **24** corresponding to **2** of FIG. **1** to provide chroma **27**, PLL **30** of the type described in U.S. Pat. No. 4,026,041 responsive to furst flag **28** from sync separator **25** for generating a sampling clock **31** which is phase locked to the color burst, which sampling clock is coupled to an A–D convertor **26** which digitizes the composite video input to provide a digitized video stream **29**, shown to be a single line connection, however one skilled in the art will understand that the single line connection as well as the single element circuits which are shown herein represent multiple digital elements and connections. Digital video **29** also connects to FIR BPF (Finite Impulse Response Band Pass Filter) **33** corresponding functionally to **24** and to **2** of FIG. **1**, FIR LPF **34** corresponding to 4 of FIG. **1** to provide Luma **30**, FIR BPFs **38** and **39** corresponding to **13** and **14** of FIG. **1** and providing R-Y **40** and B-Y **41**, and Matrix **42** corresponding to **23** of FIG. **1**. In this prior art example, since the sampling clock is phase locked to the color burst of the video signal, and the frequency is chosen to be 4 times the subcarrier frequency, the four samples per subcarrier cycle then correspond to the four quadrature phases of the reference subcarrier. The sampling clock may then be divided by 2 by element **32** and coupled to a suitable switch **37** to alternately apply the digital chroma samples (with appropriate polarity inversion by the switch) to the color difference low pass filters **38** and **39**. This system is fairly complex by virtue of the stringent phase locking requirement of the sampling clock which is placed on **30**. The system is not suitable for use in heterodyne color systems such as used in home video recorders. In heterodyne color systems, the color subcarrier frequency is not phase locked to the video sync horizontal frequency. In order to perform any digital video processing, such as image manipulation, it is desirable to have the sampling clock phase locked to the horizontal sync. Since in heterodyne color systems the color subcarrier is not phase or frequency locked to sync, it is not possible to have the sampling clock **31** phase or frequency locked to both sync and color burst by **30**.

FIG. **3** shows yet another prior art chroma demodulator which utilizes an A–D **44** to digitize composite video **43** providing digitized video **45** corresponding to **26**, **1** and **29**, respectively of FIG. **2**, BPF **46** providing digital chroma **50** corresponding to **33** and **35** of FIG. **2**, LPF **48** providing Y signal **54** to Matrix **66** corresponding to **34**, **36**, and **42** of FIG. **2**, and color difference LPFs **62** and **63** corresponding to **38** and **39** of FIG. **2**. Additionally, FIG. **3** shows a digital sync separator **47** which provides H sync **52** to a digital PLL **49** which generates an H locked sampling clock **53** which the A–D **44** utilizes for sampling the video. Element **7** also provides BF **51** which is coupled to a second digital PLL **55** to provide digital quadrature reference signals **56** and **57** in response to chroma subcarrier reference burst of **50**, which reference signals are multiplied with chroma **50** in multipliers **58** and **59** to provide the R-Y and B-Y signals **60** and **61** which are coupled to **62** and **63** providing filtered R-Y **64** and B-Y **65**. This prior art circuit overcomes the problem of operating with heterodyne color but at the expense of a second PLL **55** which adds to the expense of the circuit which is already impacted by the first digital PLL **49**. In addition, it is difficult to achieve an accurate phase lock with PLL **55**, which is most commonly implemented with a crystal oscillator at some high frequency, usually around 30 MHz, and a numerically controlled oscillator (NCO). The NCO requires a fairly large accumulator in order to achieve phase lock accuracies which typically need to be within 1°.

SUMMARY OF THE INVENTION

This invention includes a novel reference measurement circuit which samples and measures the carrier reference's phase and/or frequency relative to the discrete time sampling. The invention includes a demodulator reference signal generator to generate properly phased reference signals in response to the sampling to carrier reference phase and frequency. The reference signals are for use by a phase demodulator circuit. Novel methods of computing the sampling to carrier reference phase, generating the reference signals, demodulating the modulated carrier and filtering the demodulated signals are also shown. The invention is particularly useful for decoding chroma difference signals of

PAL and NTSC television video signals.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. **1** shows a prior art analog R-Y, B-Y chroma demodulator and PLL with RGB matrix.

FIG. **2** shows a prior art digital RGB chroma demodulator with an analog PLL.

FIG. **3** shows a prior art digital RGB chroma demodulator with a digital PLL.

FIG. **4** shows a first embodiment of the invention.

FIG. **5** shows a detailed diagram of **84** and **94** of FIG. **4**.

FIG. **6** shows a trigonometric relationship of color burst and sample points.

FIG. **7** shows a detailed diagram of parts of **84** and **94** of FIG. **4**.

FIG. **8** shows a digital demodulator using logarithm type processing circuits.

FIG. **9** shows a digital finite impulse filter using logarithm type processing circuits.

FIG. **10** shows a digital embodiment of **97** of FIG. **4**.

DESCRIPTION OF THE PREFERRED EMBODIMENT

The description of the preferred embodiment of the present invention is given as used for a chroma decoder for NTSC like color signals. The terms sample and pixel , encode and modulate, decode and demodulate, as well as burst and reference, subcarrier and carrier are used somewhat interchangeably in the present description, as is typical in the video art. One skilled in the art will recognize from the descriptions and teachings herein, taken in conjunction with the drawings and claims, that the inventive concepts will apply equally well for operations with other types of signal demodulation etc., for other industries and technologies. It will be understood that other arts will use different terminology than that used for the description herein, which may apply to other arts without respect to the particular terminology used in the particular art. For example, this invention could be used for digital modem circuitry which decodes digital data on phase and amplitude encoded carriers used for transmission over analog channels such as telephone circuits, microwave links, radio frequency communications and satellite transponders.

In the present disclosure, the particular term which is conventionally used in the present video related technology or art, is intended to imply and include the functional equivalent which may be identified by a different terminology in the same or different technology.

The invention described herein is practiced using basic functional components such as adders, subtracters, accumulators, registers, logic elements, look up tables and filters. The description of the preferred embodiment is given for digital circuitry, however one skilled in the art will recognize from the teachings that the invention may also be practiced utilizing analog circuits. In addition, it is believed that one skilled in the art will be quite capable of selecting appropriate integrated circuits, or of designing such functional components from circuits and components which are readily available. In particular, integrated circuits which are manufactured by Analog Devices, Norwood, Mass., Brooktree, San Diego, Calif., TRW Inc. of La Jolla, Calif., Integrated Device Technology, Santa Clara, Calif., and Motorola, Austin, Tex. may be used, and one is referred to application notes, technical specifications and other literature which is available from these manufacturers.

Particulars of implementation of digital video related filters, PLLs, Sampling, A–D conversion, as well as descriptions and teachings of the basic circuit elements found herein may be found in a number of reference materials. In particular, the *Society of Motion Picture and Television Engineers Journal* and *D·I·G·I·T·L Television* edited by C. P. Sandbank, published by John Wiley & Sons, New York, N.Y. 10158 are especially good sources.

In the drawings and descriptions of the various embodiments of the invention given herein, it is assumed that those reading the disclosure are skilled in the art and will appreciate the details of construction from the drawings and descriptions given. In particular, as is common in the art, detailed information, for example polarities, signs of combination in adders or multipliers, phases of combined signals, etc. will not be shown, as one skilled in the art will recognize and provide for such detail in practicing the present invention. For example, in FIG. **3**, element **21** is shown as simply a "-" block. One skilled in the art will realize from the teachings herein, that this block is intended to subtract the R signal and subtract the B signal from the Y signal.

FIGS. **1–3** show prior art versions of chroma decoders as discussed above.

FIG. **4** shows a first embodiment of the present invention for providing three color outputs from a composite video input **67**. The preferred connection of elements is shown in solid lines, with other embodiments which are reasonably expected to be of commercial value shown by dashed lines. In the preferred embodiment, a sync separator **69** having input **76** responsive to input video **67** provides a Burst flag signal (BF) **74** and a Horizontal sync signal **75** (H) both in response to the composite video sync as is well known in the art. An H locked PLL **70** generates a sample clock which is phase locked to H sync, which sample clock is utilized by A–D convertor **68** to sample input video **67** thereby providing digitized composite video **73** which in the preferred embodiment is an 8 bit digital signal as is well known in the art. The Brooktree Corp. sells a module, the AD9502, which performs the functions of **68**, **69**, and **70**, receiving a video input and providing a clock and digitized video out. The 8 bit digital video **73** will be shown as a single line for clarity, however it will be understood that this and other parallel digital signals are to be suitably coupled as represented by single line connections and single element components.

Alternatively, a burst locked PLL **72**, responsive to BF **74** and Chroma **79**, such as described in U.S. Pat. No. 4,062,041, could be used to generate the sampling clock **77**, however as will be appreciated from the present disclosure such is not necessary and would incur additional expense. The burst PLL would be incorporated by making alternate connections **81A** and **81B** in place of connections **80A** and **80B**. Further, it will also be appreciated that a free running, or gated free running sampling clock may also be utilized, however this is not as desirable as the suggested H locked sampling clock.

For the purpose of the present example, and as chosen for the preferred embodiment, the sampling clock **77** is phase locked to horizontal at a frequency which is chosen to be nominally 4 times the color subcarrier frequency. Other frequencies may be used as well, however this relationship finds considerable acceptance as a standard. For NTSC video, the sampling clock will be at a frequency of 910 H, or 14.3 MHz. For PAL, the sampling clock will be 1135 H

or 17.7 MHz. Other frequencies and ratios may be utilize with minor changes to the circuitry to accommodate them as will be apparent to one skilled in the art from the present teachings. Alternatively, the sync separator **69** may be coupled to digitized video **73** instead of analog video **67**, by making connection **81C** in place of **80C**, and a burst PLL **72** may be utilized to generate a burst locked sampling clock **78** which is substituted for the H locked clock **77** via connection **81B**, which burst PLL operates in response to chroma **79** from analog chroma BPF **71**, or digital chroma **83** from digital chroma filter **82**, and in further response to burst flag **74**, all as is well known in the art.

The chroma demodulator of FIG. **4** contains digital chroma band pass filter **82** responsive to digital video **73** to provide digital chroma **83** which may optionally be delayed by delay **15D**, subtracter **88** to subtract digital chroma **83** in either direct or optional delayed form from digital composite video **73** to provide digital luma (Y) **89**. Such filters are well known in the art, such as that described in U.S. Pat. No. 4,803,547. The Motorola MC141620 is also suitable for low performance analog consumer applications. Demodulator **90** containing multipliers and low pass filters corresponding to **58**, **59**, **62** and **63** of FIG. **3**, is responsive to digital chroma **83** and reference signals **95** and **96** to provide demodulated difference signals **92** and **93** as is well known in the art, with FIG. **4** further containing matrix **91** similar in function to **66** of FIG. **3**. The Brooktree BT**281** is one such matrix which is suitable for this operation.

FIG. **4** further shows a novel chroma reference generating means **97** responsive to burst flag **74**, sample clock **77**, digital chroma **83** (of which only the reference burst is used), optional phase adjustment **114** and providing a plurality of reference outputs **95** and **96**, which in the present example and preferred embodiment are chosen as SIN ϕ and COS ϕ where ϕ is the color burst phase from color burst of **83** offset by the amount of phase adjustment **114** (if any). Demodulator **90** will then output color difference signals **92** and **93** such as I and Q or R-Y and B-Y depending on the setting of **114**, which may also be used as a tint control for NTSC signal demodulating. Novel chroma reference generating means **97** contains a burst to sample clock ϕ and frequency offset detector **84** which measures the relative burst to sampling clock phase for each color burst, and outputs this value **86**, and additionally may measure the sample to sample burst ϕ increment (relative to burst) value which is output as **87**. The ϕ measure **86** and ϕ increment **87** values are coupled to the chroma reference counter **94**, along with sample clock **77**, burst flag **74**, and phase adjustment **114** and, as required, timing and control signals **85**. For each sample of chroma **83**, chroma reference generator **94** outputs the appropriate plurality of reference signal values **95** and **96** to enable the demodulator **90** to operate properly. More than two signals **95** and **96** may be output if needed. The Novel chroma reference generating means **97** has the particular advantage of operating without PLL's or NCO's and will operate to properly supply reference signals **95** and **96** with heterodyne chroma and H sync locked, or even free running or gated free running sampling which is one of the features of the present invention. For example, **97** could be utilized with a sampling clock generator such as described in U.S. Pat. No. 4,999,526.

FIG. **5** shows a detailed diagram of an embodiment of the novel chroma reference generating means **97** of FIG. **4**, including **84** and **94** of FIG. **4**. The sign bit of digital chroma **83** is coupled to one input of gate **103**, and through the latches **98***a*, **98***b*, and **98***c* with the output of each latch also coupled to gate **103**. The digital chroma **83** is coupled to latch **98***g* and to divider **99**. The output of **98***g* is also coupled to divider **99**. The output of divider **99**, which represents the TANGENT of α which is the sampling to burst angle of the current sample, is coupled to the input of ARCTANGENT calculator **100**. ARCTANGENT calculator **100** outputs the sampling angle α **154** which is coupled to the inputs of latches **98***e* and **98***f*. The output of **98***e*, X, is coupled to subtracter **101**, and the output of **98***b*, Y, is coupled to subtracter **101** and is also output from **84** as the phase measure **86**. The output of subtracter **101** is X-Y and represents the phase change of 8 cycles of burst over 32 samples. Circuit **102** is labeled as ÷32 for simplicity, however in **102** the value X-Y is added to 8·360° and the sum is divided by 32. Circuit **102** thus computes the value which represents the average burst phase change over each sample, and this is output from **84** as the sampling phase increment value **87**. Note that the difference of values X and Y represent degrees of subcarrier deviation over 8 cycles of color burst subcarrier, therefore even if X-Y is zero, the divider **102** must recognize that 32 samples were made over 8·360° therefore the ϕ increment value 87 will be 90°, not 0°. That is why **102** divides by 32 samples per 8·360°. In the present example the value of [(X-Y)+(8·360°)]÷32 is added to 90° to yield the value 87. It should be noted that it is intended for the first and 32nd sample to both occur in the same slope half cycle of the burst, that is they both should be from the half cycle defined by the fourth and first quadrant, or from the second and third quadrant. If the frequency difference between the sampling and the burst is such that the 32nd sample does not occur in the same slope half cycle from the 8th burst cycle, the value of 8·360° and associated calculation must be modified accordingly to reflect the half cycle which the 32nd cycle occurs in. The number of half cycles is counted by **157** and coupled to **102** as **158**.

Gate **103** which has as its inputs the sign of the previous 3 and current samples performs a subcarrier quadrature identification function. When the sample signs are in the sequence − + + −, **103** outputs a rising edge **108** which clocks latch **104**. This rising edge identifies when the current sample is being made in a known quadrant corresponding to a known slope half cycle of the subcarrier. For applications where there may be a large frequency difference between the burst and the sampling, an adder **157** should be combined with the output of **103** to keep track of the number of like sloped half cycles **158** which are sampled during the 32 samples. Burst flag **74** is used to hold **104** clear, except during burst so that the output of **104** will go high at the time period when sample C of FIG. **6** is present at **85**. This will allow the value of α for sample A to be latched into **98***e*. This value is the value of the first sample of the first positive half cycle of the color burst. Note that ARCTANGENT circuit **100** will contain a clock delay so that e is present at the input of **98***e* when **108** clocks **98***e*. Output **108** also enables 32 counter **105** which is held clear by BF except during the burst time. Counter **105** outputs a clock signal **109** 32 counts into burst flag to clock the value of α corresponding to the first sample of the eighth positive burst cycle into latch **98***f*. The sample clock **77** is appropriately coupled to the various registers, latches, etc., in order to provide proper clocking.

The sample phase **86** and the sample to sample phase increment value **87**, as well as the 32 counter output signal **109** are coupled to the reference generator circuit **94**. Phase offset value **114** is added to **86** to offset that phase value by an amount suitable for changing the demodulation angle of the reference signals, or alternatively to adjust the tint of the demodulated signal as is common for NTSC demodulators.

The phase offset may also be adjusted at **107B** as indicated by the dashed connections. Switch **106** is caused to select the adjusted phase value from **113** at the proper time to acquire the newly computed value in response to signal **109**. At the next clock that value is incremented by the phase increment value **87** by the phase accumulator comprised of register **98D** and adder **107A** with the output of **98D** coupled through **106** to **107A**. Consequently, the incremented phase value from **107A** will match each new sample's phase as that sample is present. The phase value for each sample is coupled to the SIN and COS look up tables **111** and **112**, via **107B** if used, where the proper SIN and COS value for each phase applied is output on **95** and **96**. The reference signals **95** and **96** are coupled to the chroma demodulator **90** of FIG. **4**, where they are multiplied with the modulated chroma subcarrier in order to demodulate the subcarrier into color difference signals **92** and **93**.

FIG. **6** shows the trigonometric relationship as applied to color burst and sample points and which is used to explain the operation of the present invention. A typical color subcarrier burst sine wave is shown with sample points A through H indicated and further showing angular relationships **115** and **116**. A detailed view of sample points A & B on half cycle **117** is shown. Trigonometric formulas relating the circuit operations of FIG. **5** are given with respect to the sample points A through H. Since the sample value of A is equal to the SIN of the sample angle α multiplied by the amplitude of the sine wave at that sample point, and sample value B correspondingly responds to COS α, then the angle α can be computed from the sample values A and B independent of any overall amplitude gain change of the signal. The TANGENT of α is simply the ratio B/A which is computed by **99** and **98***g* as shown in FIG. **5**. ARCTANGENT calculator **100** is used to arrive at the angle α from its TANGENT. In the preferred embodiment, **100** is simply a digital PROM or ROM which contains the appropriate angle for every possible TANGENT which can be provided with a number of digital bits output from **99** of FIG. **5**, which in the preferred embodiment is 9 bits. The 9 bits of angle TANGENT gives **512** angle TANGENTS for 512 angles between 0° and 90° which achieves better than 1° resolution. Note that the 512 angles are not equally divided into 90°.

The angle of sampling on a cycle of the subcarrier reference signal is thus calculated for a known sample by trigonometrically operating on one or more pairs or a plurality of samples. The sample to sample phase change is also calculated. Reference signals are generated in response to the sample to sample phase change by incrementing the reference generator by the same phase change. The phase of the reference generator may be checked against the calculated phase for a known sample, and corrected accordingly if it is in error by a predetermined amount, or alternatively the calculated phase for a known sample can be substituted for the phase of the reference generator. As an additional feature of the present invention, the past history of the error between the calculated phase and the actual phase of the reference carrier can be used to predict the upcoming error with better accuracy. Further, in systems where the chroma frequency changes between color bursts, or where the sampling clock frequency is changing between color bursts, the burst to burst error can be used as a modulation factor, to frequency modulate the generation of the reference.

FIG. **7** shows a detailed diagram of parts of **84** and **94** of FIG. **4**, which diagram includes improvements and alternate embodiments to **84** and **94** shown in FIG. **5**. FIG. **7** shows a more accurate method of calculating the ϕ increment value **87** and the ϕ starting phase value **86** of FIGS. **4** and **5** as compared to the method of circuit elements **98***b*, **101** and **102** of FIG. **5**. Elements **125**, **126**, **118**, **119** and **127** of FIG. **7** therefore replace elements **101** and **102** of FIG. **5**. Elements **120**, **121**, **122**, **123** and **124** of FIG. **7** then replace **98***f* of FIG. **5**.

FIG. **7** shows the measured sampling phase α **154** taken from **100** of FIG. **5**, as input to **98***e* as in FIG. **5**, but having new subtracter **125** to which α is also applied. The other input of **125** is the output of **98***e* which is α delayed by 1 clock, with the output of **125** being applied to an accumulator constructed of **126** and **118**. The delayed α from **98***e* is also applied to the accumulator composed of **122** and **124**. The first accumulator **126** and **118** is held clear by BF except during burst where the accumulator is allowed to accumulate 32 values of the difference of α from sample to sample. This accumulated total of the sample to sample differences is then divided by 32 in **119**, thus becoming the average sample to sample ϕ increment value over the 33 samples (corresponding to 32 sample to sample differences), which are taken over the burst. After the 32 sample differences are accumulated and divided, this average value is latched in register **127** by the 32 count from counter **105** of FIG. **5**.

The use of accumulation and divide calculates the average ϕ increment value and allows any errors from random noise or sampling phase jitter to be correspondingly reduced. This feature is of considerable value for allowing proper operation of the demodulator with noisy or otherwise less than perfect digitized video signals and is one of the inventive features of the present disclosure.

The color subcarrier reference is sampled at known times to produce a set of digital or analog samples representative of the subcarrier reference. The set of samples is operated on via digital or analog circuitry so that the sample to sample phase change is processed over a number of samples of burst to give a value which is statistically descriptive of the phase change parameter of the set of color subcarrier reference samples. The processing of sample to sample phase change values is preferred to be integration or averaging. In the present embodiment, the representative value of the sample to sample phase change is utilized by the reference generating circuit to generating the demodulator reference signals which are multiplied by the modulated chroma subcarrier.

As will be realized by one skilled in the art from the present disclosure, several other values which are statistically descriptive of a parameter of the set of samples taken over the burst period may also be used. The set of samples may be just 2, as in the operation of **98***e*, **98***f* and **101** of FIG. **5**, however it is preferred to use 32 or more such as in FIG. **7**. By way of example, any of the various integrals, means, the mode or the median, a quartile, decile, percentile, any of the various deviations, etc. may be suitable for use in particular embodiments which are tailored to achieve specific performance in the presence of specific types of artifacts or degradation. The average has however been found quite preferable for the preferred embodiment, with the integral and median also being envisioned as quite suitable.

One skilled in the art may wish to refer to statistical texts, such as the section on Probability and Statistics from the latest "CRC Standard Mathematical Tables" published by the Chemical Rubber Co. of Cleveland, Ohio 44128 for descriptions of various methods of computing values which are statistically descriptive of sets of samples or values.

Integrating or averaging the sample to sample phase change is relatively easy, in view of the value being the same for each sample. The value is expected to be constant by virtue of the preference that the color subcarrier and sam-

pling frequencies be fixed, though not necessarily harmonically related. The other value which is used by the reference generator circuit **94** of FIG. **7**, is the starting phase value **86** which represents the sample phase at the start of each color reference subcarrier burst. This value is used by the reference signal generator as a known value which it must be set to, or checked against to ensure consistent and correct phase of the reference signals which it generates. As with the sample to sample phase change **87**, it is desirable to sample the color subcarrier reference at known times to produce a set of samples representative of the subcarrier reference. The set of samples is operated on so that the equivalent sample phase for each sample is integrated or averaged over a number of samples of burst to give a value which is statistically descriptive of the equivalent phase parameter of the set of color subcarrier reference samples. In the present embodiment, the sample to sample phase may in fact change, there being no requirement that the sampling be phase locked to the color subcarrier burst. Averaging or integrating the sample to sample phase over a number of samples therefore becomes somewhat more of a problem than integrating the sample to sample phase change. The circuitry **120** through **124** accomplishes this task, obtaining a value which is representative of an averaged value, but corresponding to the precise noise free value of a particular sample, which is the representative value utilized by the reference generating circuit in generating the demodulator reference signals which are multiplied by the modulated chroma subcarrier.

The accumulator made up of **122** and **124** is held clear by BF **74** until the reference burst samples are present at the output of **98***e*. The accumulator operates in a modulo 4, requiring 4 register sections in **124**, since there are approximately 4 samples taken for each cycle of reference burst. The accumulator therefore accumulates the value of each phase for each one of the 4 samples associated with a color subcarrier cycle. For example, referring to FIG. **6**, sample A from the first quadrant is accumulated with the fourth sample, the eighth sample, etc. through sample F, the 32nd sample. In the preferred embodiment which operates with NTSC video, there are approximately 8 cycles of burst, and burst flag (BF) identifies 8 cycles, after 32 samples, **122** will output the accumulated value of the first quadrant samples of the 8 cycles of burst. The accumulated value is divided by 8 in **121** giving the average value of the first quadrant sample over the 8 cycles of burst. It has been presumed by way of example that the A sample lies in the first quadrant, however this is not a requirement, thus the A sample may lie in any quadrant. Additionally, there is no need for the A sample to remain in any given quadrant over the 8 cycles of burst. If in fact there is a frequency difference between the samples and burst such that successive samples are other than 90 degrees apart, the average value output from **121** at the end of the 32 samples will represent the instant value associated with the start of the middle burst cycle, that is the 5th cycle of burst, which is also the 17th sample.

As a quick example, assume that the sample to sample difference corresponds to 95 degrees of subcarrier burst. Assume that sample 17 corresponds to a value representing 0°. The 13th sample will be −5° and the 21st sample will be +5°. The average will be 0°. One skilled in the art will recognize that this average mechanism will operate properly even though the sample frequency is substantially different than precisely 4 times the subcarrier frequency.

Additionally, one skilled in the art will also be able to modify the circuitry from the teachings herein to allow operation with other nominal sampling to subcarrier frequencies. Such modification may be effected by replacing **124** with a tapped shift register where the output tap which is selected to feed the stored value back to **122** is changed in response to the sampling clock to burst frequency. Such selection may be automatic, or under operator control. Automatic selection may be accomplished by counting the average number of burst samples having positive values, and selecting the tap giving twice that number of delay stages. In the preferred embodiment described herein, there are 4 samples per burst cycle, therefore there are two consecutive positive cycles and the tap of **124** would be selected to provide 4 delay stages. This inventive feature will be easily implemented by those skilled in the art using standard logic elements.

Since the output of **121** represents the phase value for the 17th sample, and the value 87 is not available until the 33rd sample is present at the input of **98***e*, it is desirable to add the accumulated phase change from the 17th to the 33rd sample to the value in **121** in order to arrive at the value for sample 33. This added value is 16 times the sample to sample phase change which conveniently is available at **119**. Multiplier **120** multiplies the value from **119** to generate this correction factor, thus providing value **86** from **123**. Alternately, the correction value may be derived directly from **126** by simply bit shifting, or from **119** as a second output. It is also possible to eliminate this **123** and **126** operation, since only a static error is picked up by such elimination, and the static error may be removed by adjusting **114**.

Additionally, it should be noted that if the sample to sample phase change is expected to always be constant, a fixed value representing 16 times this expected value may be added to the output of **121**. Further, if the sample to sample phase change is expected to be constant, this eliminates the need for **125**, **118**, **119**, and **127**, and this fixed expected value may be substituted for **87**.

Once the value of the sample to sample phase change **87** and the phase of a given sample of the reference burst **86** are arrived at or computed, they are applied to the reference signal generator **94**. Reference generator **94** is an accumulator comprised of **107**A and **98**D where the previous sample phase value **110** is incremented at every clock cycle by **107**A (that is **107***a* adds phase in modulo 360°) by the sample to sample phase change **87**. This operation gives the phase of the reference subcarrier signal for each and every sample. At the start of each line containing a new color burst, switch **106** causes the new sample value **86** to be loaded into the accumulator, this action in response to the 32 count signal **109**. In order to allow a static phase adjustment to provide for demodulation along a particular axis, and/or to provide for a tint control as is common in the art, an offset phase value **114** is added to the present sample phase by **107***b*, which is also a modulo 360° adder. The angle value corresponding to the offset reference carrier phase for each sample, which is output from **107**B, is then coupled to SIN and COS look up tables (LUT) **111** and **112** which output the value of SIN and COS on **95** and **96** corresponding to the angle of the present sample offset by **114**. The values **95** and **96** are those utilized by the demodulator **90** of FIG. **4** and which are multiplied with the color subcarrier to accomplish demodulation.

FIG. **8** shows an alternate embodiment **90'** which may operate in digital or analog form but which is preferred to be implemented in digital form, including **90** of FIG. **4** which has cost and performance advantages over the prior art method when utilized with the circuit of FIG. **7**. Since it is desired to generate reference subcarrier values to be multiplied with the modulated subcarrier, elements **107**B, **111**,

112 and the multipliers normally found in 90 with the circuitry of FIG. 8. The ϕ signal 110 from 98D is applied to LOG SIN and LOG COS look up tables 128 and 129 which output the LOG of the SIN and COS values for each phase value. Since multiplication of signals can be accomplished by adding logarithms, the LOG of the digital chroma subcarrier from 132 is added to the LOG SIN and LOG COS in adders 130A and 130B. The resultant signal which corresponds to the LOG of the demodulated chroma difference signal is converted back to normal and low pass filtered, with LOG^{-1} low pass filters 131*a* and 131*b*, thereby providing the filtered color difference signals 92 and 93. Since it is desired to convert the digital chroma to LOG chroma 83' by LOG LUT 132, the operation of computing TANGENT α and α may be simplified to replace divider 99 of FIG. 5 with a subtracter. The circuit which computes α via logarithms is comprised of 98G', 99' and 100' of FIG. 8, which divides the current and past sample values by subtracting the LOG of the samples 83'. The resulting LOG TANGENT value out of 99' is then converted back to α by the ANTILOG, ARCTANGENT look up table 100'. The additional function of ANTILOG which is included in 100' does not increase the size or cost of this element, it merely requires that the PROM be loaded with different data.

FIG. 9 shows the preferred embodiment of LOG^{-1} LPF 131A and 131B of FIG. 8. The LOG of the demodulated chroma difference signal is input at 133, coupled to an antilog LUT 134A, and the inputs of a plurality of coefficient adders 136A through 136N. The coefficient adders add the LOG of the filter tap coefficients 155A– 155N to the log input signal from 134A held in latch 135A, which is equivalent to multiplying the demodulated chroma difference signal by a filter tap coefficient. The outputs of the coefficient adders 136A through 136N are coupled to antilog LUTs 134B through 134N+1 respectively, thus making all of the tap values available for registers 135B through 135N+1 and 138M. The tap values are then shifted and summed as for example by 137A, 138A, and 137N to generate an output signal, as is normally done with digital filters.

Moving to FIG. 10, one skilled in the art will recognize that often the sampling frequency will be constantly changing. Such will be the case when the video signal contains timebase error and the sampling clock phase locked to H. In the case of heterodyne color, the color subcarrier frequency will be relatively constant, but because the sampling frequency is constantly changing in response to timebase error, an error of the generated reference signal will always be present at the next line burst, even if the sample to sample phase value were to be updated correctly for the present line. This situation also exists for PAL signals where the color subcarrier is not exactly a multiple of the video H sync rate. This is commonly referred to as the 25 Hz color subcarrier offset. The problem of having color subcarrier to sampling clock frequency changes can be overcome by predicting the phase error for the next line. The prediction is used for correcting the present sample to sample phase increment value to cause the error which would have been generated to be absorbed over the line on a sample by sample basis.

For example, at the time of a current burst it can be known or predicted that the error of the generated reference will be some value, say 10 degrees, at the next burst. The generation of the reference can be altered to correct the error during the upcoming line by distributing the 10 degree error over all of the upcoming generated samples. The future prediction can be easily achieved by delaying the chroma subcarrier, 83 of FIG. 4, by 1 H at the input of the demodulator 90. Stated another way assume line Y follows line X. The phase error of the generated reference to line X burst is 0. The phase error of the generated reference to the line Y burst is 45°. Assume there are 100 samples per line. The per sample error over line Y is therefore 0.45°. The value 87 corresponding to a sample to sample phase change is then changed by the 0.45° error by the action of 84. Normally this would not occur until after line Y where the error actually took place, however by delaying the line Y chroma subcarrier by one line before decoding, this error will be canceled by the new sample to sample phase value 87. In effect, delaying the chroma subcarrier before decoding is allowing prediction and correction of the phase error before it is used for decoding. This effectively results in frequency modulation of the generated reference.

FIG. 10 shows another embodiment of 97 which may operate in digital or analog form but which is preferred to be implemented in digital form, with the logarithm processing in 84, and with a different accumulator and reference generator configuration for 94 as compared to FIG. 5. Digital chroma 83 is input along with the sample clock on 77 and burst flag on 74. Digital chroma is converted to logs 144 by 138 and the TANGENT taken by 139, 141 and 140 giving the LOG TANGENT ϕ 142, which is then converted back to ϕ by 143. One will recognize that this circuit 84 operates in a manner similar to the bottom part of FIG. 8. The sampling angle ϕ, 86 which is not averaged, is coupled to the A input of subtracter 145. Subtracter 145 calculates the difference between the measured sample phase 86, and the accumulated sample phase from accumulator 107A and 153 which is latched into latch 159 by burst flag. This value A–B represents the error between the accumulator phase value and the measured value, which should be zero if the accumulator is operating properly and the sampling frequency is constant. If however, the sampling frequency is changing, an error is generated by 145. The error A–B is multiplied by a percentage by 146 to give a percentage error 152, which is accumulated during burst by accumulator 147 and 148 via connection 150. Latch 148 is clocked by the gated sample clock 156 from gate 149 which gates the sample clock through during burst flag. At the end of BF, the sample clock is gated off by 149, and the last accumulated sample to sample phase change value 151 is held by 148. During burst flag, switch 160 is caused to input the instant sample phase to 153, in effect resetting the accumulator to zero error.

The percentage in 146 is chosen to be a value which divides the error by the number of samples line to line, times the number of clocks 156. In this fashion, the value 151 will be averaged over the number of values 86 which are calculated during burst flag, and divided by the number of samples per line, thus giving the sample to sample portion of the line to line phase error. Thought of another way, 151 is the sample to sample phase change due to the frequency variation of the sampling clock.

The second accumulator 107*a* and 153 is clocked continuously, thereby calculating the phase value for each and every sample clock 77 throughout the video line, including the values of the samples of the next burst which occur on the next line of video. When the next line burst sample values are present at A of 145, the error A–B is again measured, and a percentage of that error, if any, is added to the sample to sample phase change value 151 to arrive at a new value if an error was present.

Otherwise, if there is no error, the percentage is 0 and the old value is held in 148. The phase value of each sample from 153 is offset by a static phase 114 in 107*b*, and coupled to SIN and COS look up tables 111 and 112 to generate the reference signals 95 and 96, as in FIG. 5.

While the present invention has been shown and described by way of example in the preferred embodiment, various other combinations, variations and modifications will readily occur to one skilled in the art from the teachings herein, and may be employed to accomplish various tasks related to demodulating phase modulated signals and generating reference signals without departing from the spirit and scope of the present invention as hereinafter claimed.

What is claimed is:

1. A reference signal generating apparatus for generating a reference signal in response to a sampled carrier reference which is sampled at known sampling times, each having a sampling angle having a tangent, to produce amplitude values comprising;

phase offset means responsive to said amplitude value at each of a plurality of known sampling times for calculating a phase measure value representative of the change in phase of said carrier reference from one of said known times to the next,

phase accumulator means operable to provide said reference signal in response to said phase measure value.

2. Apparatus as claimed in claim **1** wherein a sampling means samples the amplitude of said carrier reference in response to a sampling clock to determine said amplitude value with said sampling clock having a frequency which is not harmonically related to said carrier reference by an even integer multiple.

3. Apparatus as claimed in claim **1** wherein said phase offset means determines the tangent of the sampling angle for a given known sampling time by dividing a first said known amplitude value by a second said known amplitude value to provide the tangent of the sampling angle of said given known value which given known value is one of said first or said second known amplitude value.

4. Apparatus as claimed in claim **1** wherein the tangent of the phase of said carrier reference is determined by said phase offset means at a plurality of phase times which are located within a contiguous portion of said carrier reference and wherein said phase offset means includes means for converting said tangents to said phase of said carrier reference, with the difference between said phases of said carrier reference being determined said difference being said phase measure value.

5. Apparatus as claimed in claim **1** wherein said phase accumulator operates to produce successive reference signal values by adding said phase measure value to the previous one of said successive reference signal value to produce a current one of said successive reference signal value.

6. Apparatus as claimed in claim **1** wherein said carrier reference is intermittent in time.

7. Apparatus as claimed in claim **1** wherein said carrier reference is intermittent in time and is sampled with an analog to digital convertor means to provide said amplitude values in digital form, which sampling is performed in demodulated in response to said reference signal.

8. Apparatus as claimed in claim **1**, **2**, **3**, **4**, **5**, **6**, or **7** wherein said carrier reference is a reference burst of a video color subcarrier signal having a length from 6 to 10 cycles and said sampling is performed at other than precisely 90 degree increments thereon.

9. Apparatus as claimed in claim **1**, **2**, **3**, **4**, **5**, **6**, or **7** wherein said carrier reference is contained within a color subcarrier signal of a video signal, and said known sampling times are chosen by a sampling signal generator means in response to the scanning synchronizing portion of said video signal.

10. Apparatus as claimed in claim **1**, **2**, **3**, **4**, **5**, **6**, or **7** wherein said carrier reference is contained within a color subcarrier signal of a video signal, and said known sampling times are chosen by a a sampling signal generator means in response to the scanning synchronizing portion of said video signal, and including in combination a demodulating means responsive to said color subcarrier and said reference signal to provide a demodulated signal.

11. A demodulator apparatus operable for demodulating information content of a modulated carrier, which modulated carrier has an associated carrier reference signal which may be separate therefrom, said demodulating including operating on said modulated carrier in response to at least one demodulator reference signal generated by said demodulator, said apparatus including in combination;

sampling means to sample said carrier reference at a plurality of known times thereby producing a set of a plurality of carrier reference samples,

determining means for determining a value which is statistically descriptive of a parameter of said set of carrier reference samples, and

generating means responsive to said value for generating said demodulator reference signal.

12. A demodulator apparatus as in claim **11**, wherein the carrier reference signal is continuously present at said apparatus.

13. A demodulator apparatus as in claim **11**, wherein the carrier reference signal is intermittently present at said apparatus with said sampling of said carrier reference occurring at a frequency which is not harmonically related to said carrier reference by an even integer multiple.

14. A demodulator apparatus as in claim **11**, wherein the carrier reference signal is time multiplexed with said modulated carrier signal which said sampling of said carrier reference is at a frequency which is not harmonically related to said carrier reference by an even integer multiple.

15. A demodulator apparatus as in claim **11**, wherein the sampling means is responsive to a sampling clock to perform said sampling, which sampling clock has a known phase relationship to the scanning synchronizing portion present in the signal which contains said modulated carrier.

16. A demodulator apparatus as in claim **11**, wherein said generating means generates a plurality of demodulator reference signals which have a known phase relationship.

17. A demodulator apparatus as in claim **11**, wherein said sampling means is responsive to a sampling clock to perform said sampling, which sampling clock has a known phase relationship to the scanning synchronizing portion present in the signal which contains said modulated carrier, which sampling means provides at least three samples of said carrier reference as said set, with said determining means combining said samples as part of determining said statistically representative value.

18. A demodulator apparatus as in claim **11**, including a demodulating means wherein said information content of said modulated carrier is at least partially recovered by adding a value representative of the logarithm of said modulated carrier to a value representing the logarithm of said demodulator reference signal, and further by converting the sum of such addition to a value representing the antilog of said sum, said antilog representing said recovered information content.

19. A demodulator apparatus as claimed in claim **11**, **13**, **14**, **15**, **16**, or **17** wherein said modulated carrier is a video chroma subcarrier of a video signal, and said carrier reference is the color burst signal time multiplexed with said video chroma subcarrier with said sampling means responsive to a sampling clock to sample said color burst signal at

a plurality of known times in response to said sampling clock, said apparatus further comprising,

a sampling clock generating means responsive to scanning synchronizing portions of said video signal to produce said sampling clock at a frequency which is a multiple of said synchronizing portions of said video signal,

said apparatus still further comprising demodulator means responsive to said demodulator reference signal and said video chroma subcarrier to produce at least part of said information content of said chroma subcarrier.

20. A demodulator apparatus operable for demodulating chroma difference signals of a video chroma subcarrier, which chroma subcarrier has an associated subcarrier burst reference signal time multiplexed therein, said demodulating including multiplying means for multiplying said chroma subcarrier with a plurality of demodulator reference signals generated by a reference signal means, said apparatus including;

sampling means to sample said subcarrier burst reference signal at a plurality of known times thereby producing a set of a plurality of subcarrier burst reference samples,

selecting means for selecting a descriptive value which is statistically descriptive of a parameter of said set of subcarrier burst reference samples, and

with said reference signal means responsive to said descriptive value for generating said demodulator reference signals.

21. A demodulator apparatus as in claim **20** wherein said descriptive value is representative of the sample to sample phase change of said subcarrier burst reference signal.

22. A demodulator apparatus as in claim **20** wherein said descriptive value is representative of a mean of a plurality of sample to sample phase changes of said subcarrier burst reference signal.

23. A demodulator apparatus as in claim **20** wherein said statistically descriptive value is representative of a median of a plurality of sample to sample phase changes of said subcarrier burst reference signal.

24. A demodulator apparatus as in claim **20**, wherein said demodulator means includes means for adding a value representative of the logarithm of said chroma subcarrier to each of the values representing the logarithms of said demodulator reference signals, and further converting the sums of such additions to values representing the antilog of said sums, said antilog values representing said demodulated chroma difference signals.

25. A demodulator apparatus as in claim **20, 21, 22, 23** or **24**, wherein said sampling means also samples said video chroma subcarrier to provide a set of chroma samples, and said reference signal means includes means for generating a reference phase value for each of said chroma samples, and further including means responsive to said reference phase value to provide said plurality of demodulator reference signals.

26. A demodulator apparatus as in claim **20, 21, 22, 23** or **24**, wherein said sampling means also samples said video chroma subcarrier to provide a set of chroma samples, and said reference signal means includes means for generating a reference phase value for each of said chroma samples, said apparatus further including,

means responsive to said reference phase value to provide said plurality of demodulator reference signal values for each said chroma sample, which chroma samples are multiplied in said multiplying means by each of said plurality of demodulator reference signal values to provide said chroma difference signals,

said apparatus further operative such that said sampling means performs said sampling at a rate responsive to the synchronizing portions of said video signal.

27. The method of generating a decoding reference signal phase locked to a carrier reference signal, including the steps of;

sampling the carrier reference signal to produce a set of samples,

finding a phase increment value representative of the change of phase of said carrier reference signal from one sample to the next,

setting said decoding reference signal to a known phase value,

incrementing said known phase value of said decoding reference by the amount of said phase increment value.

28. The method of claim **27** including the steps of determining the carrier reference signal phase corresponding to a given sample,

comparing said carrier reference signal phase to said decoding reference phase corresponding to said given sample, and if said values are not in agreement, modifying said increment value in response to the amount of difference therein.

29. The method of claim **27** including the steps of determining the carrier reference signal phase corresponding to a given sample,

comparing said carrier reference signal phase to said decoding reference phase corresponding to said given sample, and if said values are not in agreement, modifying said decoding reference phase value in response to the amount of difference therein.

30. The method of claim **27** including the steps of determining the carrier reference signal phase corresponding to a given sample,

comparing said carrier reference signal phase to said decoding reference phase corresponding to said given sample, and if said values are not in agreement, modifying said increment value and said decoding reference phase value in response to the amount of difference therein.

31. The method of claim **27** including the steps of determining the carrier reference signal phase corresponding to a given sample and,

periodically modifying said decoding reference phase value corresponding to said given sample to change it to said carrier reference signal phase value.

32. The method of generating a decoding reference signal phase locked to a carrier reference signal, including the steps of;

sampling the carrier reference signal to produce a set of samples,

computing a phase increment value representative of a mean value of the change of phase of said carrier reference signal from one sample to the next,

incrementing the phase value of said decoding reference by an amount responsive to said phase increment value.

33. The method of claim **32** including the steps of determining the carrier reference signal phase corresponding to a given sample,

comparing said carrier reference signal phase to said decoding reference phase corresponding to said given sample and,

if said values are not in agreement, modifying said

increment value in response to the amount of difference therein.

34. The method of claim **32** including the steps of determining the carrier reference signal phase corresponding to a given sample,

comparing said carrier reference signal phase to said decoding reference phase corresponding to said given sample and,

if said values are not in agreement, modifying said decoding reference phase value in response to the amount of difference therein.

35. The method of claim **32** including the steps of determining the carrier reference signal phase corresponding to a given sample,

comparing said carrier reference signal phase to said decoding reference phase corresponding to said given sample and,

if said values are not in agreement, modifying said increment value and said decoding reference phase value in response to the amount of difference therein.

36. The method of claim **32** including the steps of determining the carrier reference signal phase corresponding to a given sample and,

periodically modifying said decoding reference phase value corresponding to said given sample to change it to said carrier reference signal phase value.

37. The method of claim **32** wherein the step of sampling is in response to a sampling clock which is continuous throughout the duration of the signal which is to be decoded and,

where the step of incrementing the phase value of said decoding reference is achieved by adding said mean value to the past phase value to arrive at the new phase value in response to each sampling clock pulse.

38. The method of claim **32** wherein the step of sampling is in response to a sampling clock which is continuous throughout the duration of the signal which is to be decoded, including the further step of generating said sampling clock in response to a portion of synchronizing information which is present on said signal which is to be decoded.

39. The method of determining the sample to sample change of the phase of a sampled carrier reference including the steps of;

sampling said carrier reference to produce said samples, determining the phase value of a first known sample from a known slope half cycle of said carrier reference,

determining the phase value of a second known sample from a known slope half cycle of said carrier reference,

determining the phase change of the carrier occurring from said first known sample and said second known sample,

dividing said phase change by one more than the number of samples which occurred between said first known sample and said second known sample, said result being said sample to sample phase change.

40. The method of determining the sample to sample change of the phase of a sampled carrier reference including the steps of;

sampling said carrier reference to produce said samples, determining the phase value of a first known sample from a known slope half cycle of said carrier reference,

determining the phase value of a second known sample from a known slope half cycle of said carrier reference,

determining the phase change of the carrier occurring from said first known sample and said second known sample,

dividing said phase change by one more than the number of samples which occurred between said first known sample and said second known sample,

obtaining said result number of times providing a set of results,

determining a statistically representative value for said set, said statistically representative value being said sample to sample phase change.

41. The method of decoding a color video signal to recover the color difference signals modulated on a color subcarrier therein, including the steps of;

generating a sampling clock phase locked to horizontal sync pulses of said color video signal,

sampling said color video signal with an analog to digital convertor thereby producing digital samples thereof,

filtering the color subcarrier out of the said digital samples thereby producing color samples,

producing a burst flag in response to said horizontal sync pulses,

computing a statistical representative value of the change of phase of the color burst from sample to sample in response to said color samples and said burst flag,

generating a reference phase signal from a phase accumulator,

incrementing the phase of said reference phase signal by the amount of said statistical representative value of the change of phase for each clock of said sampling clock,

offsetting the value of said reference phase by a known amount,

generating the sine and cosine values corresponding to the value of said reference phase at each new value thereof,

multiplying each of said chroma samples by said sine value and by said cosine value thereby producing unfiltered color difference signals, and

filtering said unfiltered color difference signals to produce said color difference signals.

42. The method of generating a reference subcarrier signal in response to a color video signal, including the steps of:

generating a sampling clock and in response thereto sampling said color video signal and with an analog to digital convertor thereby producing digital samples thereof;

providing color burst samples from said digital samples in response to the color subcarrier burst;

generating a burst flag in response to predetermined synchronizing pulses of said color video signal;

in response to said color burst samples and said burst flag, generating a sample phase value which is statistically representative of the change of phase of the color subcarrier burst from sample to sample;

in response to said sample phase value, generating a reference phase signal in a reference generator, for at least some of said sampling clock, said reference generator operative to increment the phase of said reference phase signal by an amount which is directly responsive to said sample phase value thus producing a data stream of reference phase signal values;

generating at least one corresponding sine value data stream in response to said reference phase signal value data stream, said data stream of said sine values representing said reference subcarrier signal.

43. In a system operating with a digitized version of an

analog signal, said system including an increment clock signal and a series of digital samples having values representative of said analog signal at the instant of taking each of said samples, said system further including reference samples having values representative of a non continuous reference signal portion of said analog signal, an apparatus for generating a series of reference values in response to said reference samples, said apparatus including:

a phase increment measure circuit responsive to said values of a plurality of said reference samples to provide a phase value responsive to the phase change of said non continuous reference signal portion over a given number of said burst samples,

a reference generator circuit responsive to said phase value and said increment clock signal which reference generator circuit provides an output signal the value of which increments in response to said increment clock signal in steps the size of which is responsive to said phase value,

a reference value circuit responsive to the output of said reference generator circuit to provide said reference values.

44. An apparatus as claimed in claim **43** wherein said phase increment measure circuit compares the sampling phase of one said reference sample with respect to the sampling phase of another said reference sample to determine the total non continuous reference signal portion phase change therebetween and a dividing circuit operative to divide the resulting difference by the number of sample periods therebetween thus providing said phase value.

45. An apparatus as claimed in claim **43** wherein said phase increment measure circuit subtracts the sampling phase of one said reference samples from the sampling phase of another said reference sample to determine the total non continuous reference signal portion phase change therebetween, and performs a plurality of said subtractions for a plurality of said reference samples, and further includes an average circuit which averages the results of said plurality of subtractions to provide said phase value.

46. An apparatus as claimed in claim **43**, **44** or **45** including a phase setting circuit responsive to one or more of said reference samples and one or more of said reference values corresponding thereto to produce an error signal representative of the error therebetween, with said reference generator circuit responsive to said error signal to reduce said error by altering said step size.

47. An apparatus as claimed in claim **43**, **44** or **45** including a phase setting means responsive to at least one selected said reference sample to produce a selected sampling phase signal therefrom, with said reference generator circuit responsive to said selected sampling phase signal to alter said phase value output therefrom in order that said reference value matches correspondingly to said selected reference sample.

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